User's Guide

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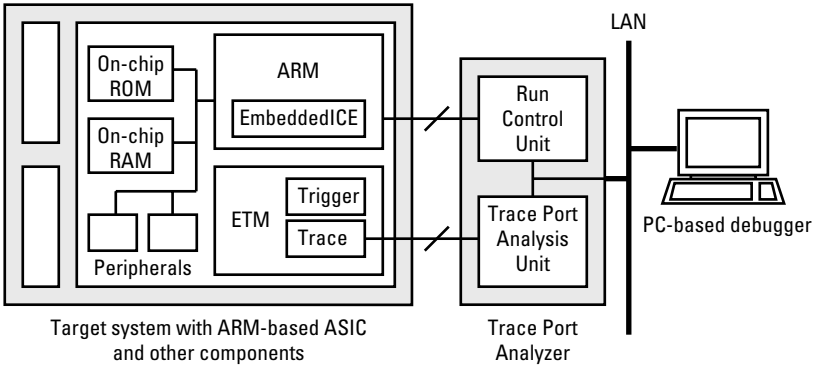
For Safety and Regulatory information,
see the pages behind the index.

Agilent Technologies E5904B Option 300 Trace Port Analyzer for ARM

ARM On-Chip Circuitry for Debugging

The ARM7 and ARM9 families of microprocessors can include an Embedded Trace Macrocell (ETM) that outputs information about processor execution to a trace port.

Software debuggers provide the user interface to the ARM ETM; they configure the trace port using a run control unit (via the JTAG interface), and they display the data collected from the trace port.



Trace Port Analyzer for ARM Overview

The Agilent Technologies E5904B Option 300 trace port analyzer for ARM contains:

- A run control unit.
- Circuitry for collecting output from the ARM ETM trace port, called the trace port analysis unit.
- A LAN interface for communicating with debuggers.

The Run Control Unit

In addition to configuring the trace port, the run control unit is also used for downloading code, starting/stopping processor execution, single-stepping through a program, setting breakpoints, and displaying/modifying registers and memory.

The Trace Port Analysis Unit

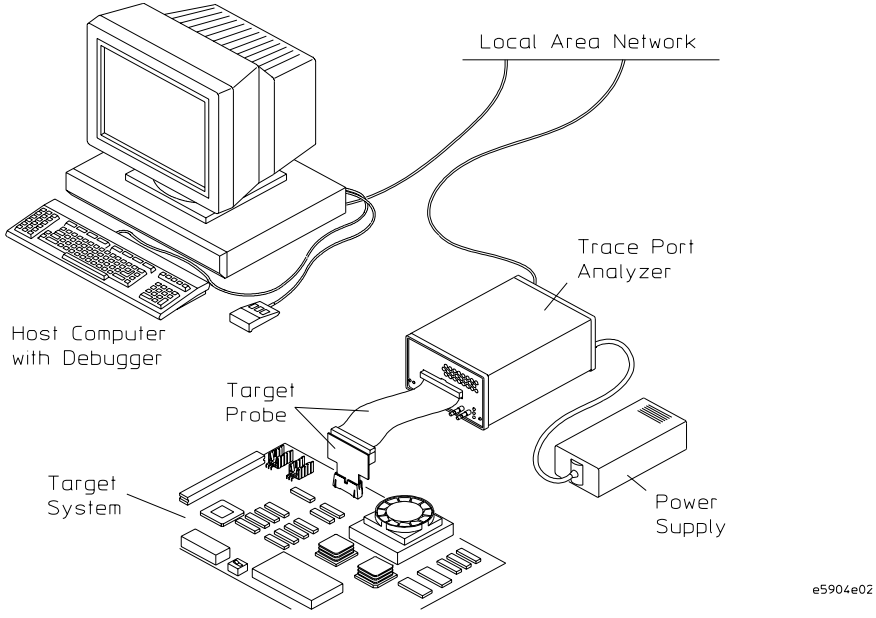
With the trace port analysis unit, you can:

- Capture ARM ETM trace data.
- Capture data on 4-, 8-, or 16-bit wide trace packet buses.
- Store up to 2M trace states with time tags off.
- Store up to 1M trace states with time tags on.
- Capture data on ARM ETM ports whose voltages are between 1.8 V and 3.3 V.
- Send a trigger signal or a run control unit status signal to other instruments, or use signals received from other test instruments to stop processor execution or trigger the trace port analyzer.

The LAN Interface

With the IEEE 802.3 Type 10/100Base-TX LAN connection, you can:

- Connect the trace port analyzer to a target system in the lab and use debuggers anywhere else on the LAN.
- Connect to either 10 Mbps (10BASE-T) or 100 Mbps (100BASE-TX) twisted-pair ethernet LANs. (The trace port analyzer automatically negotiates the data rate for the LAN it is connected to.)



Debugger Software

A debugger must be used with the trace port analyzer. Debuggers are available from ARM, Green Hills, and other companies.

The debugger user interface will let you:

- Download code, start/stop processor execution, single-step through a program, set breakpoints, and display/modify registers and memory.
- Set triggers, trigger sequences, etc., in the Embedded Trace Macrocell using the run control unit of the trace port analyzer.
- Collect trace information.
- Display execution flow and captured trace data.

Processors Supported

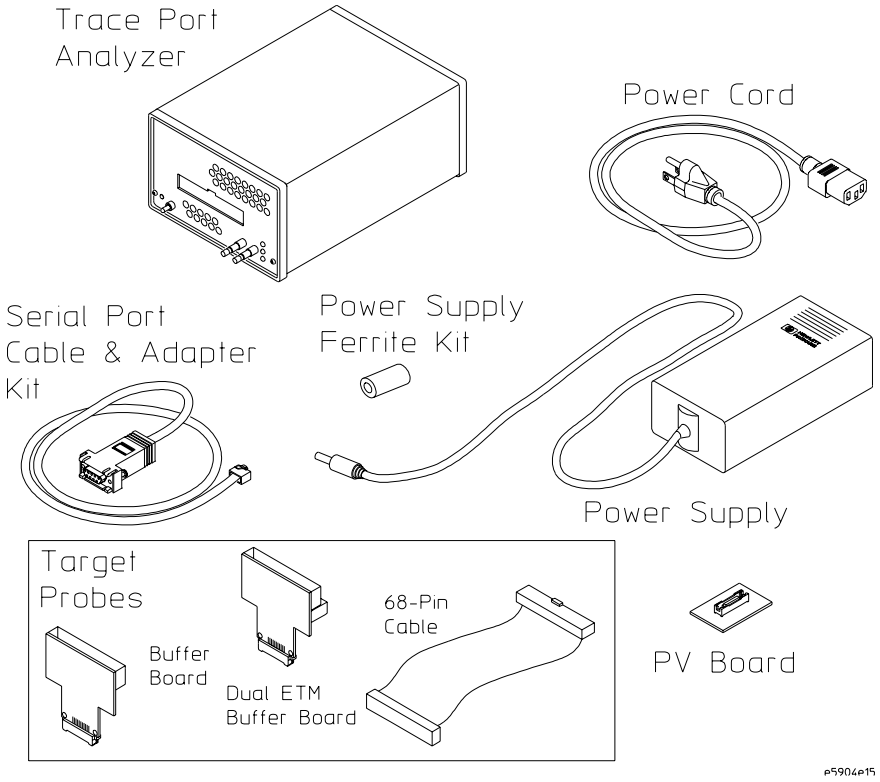
The Agilent Technologies E5904 Option 300 Trace Port Analyzer supports the following processors when they include the ARM ETM (Embedded Trace Module).

Processors Supported
ARM7TDMI
ARM7DI
ARM710T
ARM720T
ARM740T
ARM9TDMI
ARM 920T
ARM 922T
ARM 925T
ARM 940T
ARM 946ES
ARM 966ES

The Agilent E5904B Option 300 Trace Port Analyzer is designed to work with ARM ETM revision C. If you are using ARM ETM revision A or B, see “Using the Trace Port Analyzer with ARM ETM revisions A or B” on page 36.

Equipment Supplied

The Agilent Technologies E5904B Option 300 trace port analyzer for ARM consists of:



Part number	Description
0950-3043	Power supply for trace port analyzer (marked F1044B)
E3483-68700	Power supply ferrite kit
E5903-61602	68-pin cable
E5903-66507	ARM buffer board
E5903-66508	ARM dual ETM buffer board
E5903-66516	ARM ETM revision A/B buffer board - Optional, not shown. See page 36 for details.
E5903-66509	PV board
E8130-68702	Serial cable and adapter
E5904-97002	This user's guide

In This Book

This book is for the Agilent Technologies E5904B Option 300 trace port analyzer for ARM. It describes:

- Target system design considerations and other requirements of the trace port analyzer.
- How to connect the trace port analyzer to a LAN, configure it, and connect it to the target system.
- How to coordinate measurements between the trace port analyzer and other test instruments.
- How to update trace port analyzer firmware.
- How to troubleshoot and solve problems.
- Characteristics of the trace port analyzer.

See Also

The user's guide manual for your debugger.

Embedded Trace Macrocell Specification and other documentation from ARM (see the ARM web site: http://www.arm.com).

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1

Target System Design Considerations

In order to use Agilent Technologies E5904B Option 300 trace port analyzer, the ARM7/9 microprocessor must have the Embedded Trace Macrocell (ETM), and the Embedded Trace Macrocell trace port signals must be routed to a header connector in the target system.

When integrating an Embedded Trace Macrocell into an ASIC, the quality and timing of the trace port signals to the trace port analyzer are critical for reliable operation. Some of the ASIC and printed-circuit board design issues to consider are:

- Output pad selection.
- Printed-circuit board track lengths.
- Printed-circuit board track termination.
- Setup and hold times for the trace data signals with respect to TRACECLK.

The care that must be taken with the design of the trace port is generally proportional to the frequency of operation. At frequencies of more than 100 MHz careful SPICE analysis of the system, including the characteristics of the package should ideally be taken into account.

Early attention to the design guidelines can ensure correct operation of the trace port analyzer.

This chapter describes:

- A few ASIC design guidelines. Most ASIC design guidelines are available from ARM.
- Printed-circuit board design guidelines.
- The header connector and signals that should be provided by an ARM7/ ARM9 target system.
- Height restrictions and keep-out requirements.
- Timing and voltage specifications for trace port signals.
- Providing support in a target system for JTAG-only debugging.

Trace Port Signal Overview

The trace port signals consist of all of the signals provided by the ARM ETM and also the JTAG run control signals. These two groups of signals are combined onto a single connector to save space on the target system.

The trace port signals are described below.

Signals for Trace Port Analysis

TRACECLK. The trace clock signal provides the clock for the trace port. PIPESTAT[2:0], TRACESYNC, and TRACEPKT[n-1:0] signals are referenced to the rising edge of the trace clock with a single data rate trace port. When a double data rate trace port is used, these signals are referenced to both the rising and falling edges of TRACECLK.

PIPESTAT[2:0]. The pipeline status signals provide a cycle-by-cycle indication of what is happening in the execution stage of the processor pipeline.

TRACESYNC. The trace sync signal is used to indicate the first packet of a group of trace packets and is asserted HIGH only for the first packet of any branch address.

TRACEPKT[n-1:0]. The trace packet signals are used to output packaged address and data information related to the pipeline status. All packets are eight bits in length, irrespective of the number of trace packet signals implemented. There are three cases to consider for how trace packets are output on the trace packet signals:

- 4-Bit TRACEPKT Bus (TRACEPKT[3:0] signals). A packet is output over two cycles. In the first cycle, Packet[3:0] is output and in the second cycle, Packet[7:4] is output.

  TRACEPKT[15:4] signals are unused and should be connected to ground.

- 8-Bit TRACEPKT Bus (TRACEPKT[7:0] signals). A packet is output in a single cycle.

TRACEPKT[15:8] signals are unused and should be connected to ground.

- 16-Bit TRACEPKT Bus (TRACEPKT[15:0] signals). Up to two packets can be output per cycle. If there is only one valid packet, it is output on TRACEPKT[7:0] and TRACEPKT[15:8] is unpredictable. If there are two packets to output, the first is output on TRACEPKT[7:0] and the second on TRACEPKT[15:8].

EXTTRIG. EXTTRIG is an optional signal. It is intended to be an input to one of the external inputs on the ETM.

Depending on the design, ETM external triggers may not be available on the ASIC's external pins. In this case, the EXTTRIG has no function, and it is recommended that this pin is pulled to a defined state.

NOTE: This signal is important for making coordinated measurements with other test instruments.

Signals for both Trace Port Analysis and Run Control Interaction

VTref. The VTref signal is intended to supply a logic-level reference voltage to allow debug equipment to adapt to the signaling levels of the target board.

Outputs to target systems will be clamped at VTref on high level outputs. Inputs from the target system will be sensed in reference to the VTref voltage level.

NOTE: VTref does NOT supply operating current to the debug equipment.

Target boards should supply a voltage that is between 1.65 V and 3.6 V. The target board should provide a sufficiently low DC output impedance that the output voltage not change by more than 1% when supplying a nominal signal current (± 0.4 mA).

Debug equipment that connects to this signal should interpret it as a signal rather than a power supply pin and not load it more heavily than a signal pin. The recommended maximum source or sink current is +/-0.4 mA.

Signals for Run Control Interaction

VSupply. The VSupply signal is supplied by the target system. It is intended to supply operating current to debug equipment that doesn't have its own power supply. The Agilent Technologies E5904B Option 300 trace port analyzer is self-powered; it does not use the VSupply signal.

nTRST. The nTRST signal is actively driven by the run control unit to the Reset signal on the target JTAG port.

NOTE: Target board logic must ensure that there is a low pulse on the target ASIC's nTRST pin at power up.

TDI. TDI is the Test Data In signal from the run control unit to the target JTAG port. It is recommended that this pin is pulled to a defined state.

TMS. TMS is the Test Mode Select signal from the run control unit to the target JTAG port. This pin must be pulled up on the target so that the effect of any spurious TCKs when there is no connection is benign.

TCK. TCK is the Test Clock signal from the run control unit to the target JTAG port. It is recommended that this pin is pulled to a defined state.

RTCK. RTCK is the Return Test Clock signal from the target JTAG port to the run control unit. Some targets, such as ARM7TDMI-S, must synchronize the JTAG port to internal clocks. To assist in meeting this requirement, you can use a returned (and re-timed) TCK to dynamically control the TCK rate. Target systems that don't require RTCK should tie it to a fixed signal level.

TDO. TDO is the Test Data Out from the target JTAG port to the run control unit.

nSRST. This is an open collector output from the run control unit to the target system reset. This is also an input to the run control unit so that a reset initiated on the target may be reported to the debugger.

This pin should be pulled up on the target to avoid unintentional resets

when there is no connection.

DBGRQ. The DBGRQ signal is used by the run control unit as a debug request signal to the target processor. It is recommended that this pin is pulled to a defined state.

This signal is rarely implemented as a pin on the ASIC. This pin should be pulled low on the target to avoid unintentional debug requests when there is no run control unit connected.

If it is implemented, the DBGRQ signal can be used to enter debug mode after receiving a signal from another test instrument on the trace port analyzer's "Break In" SMB port. For example, a logic analyzer's triggering capability can be used for complex breakpoints.

DBGACK. The DBGACK signal is used by some run control units to detect entry or exit from the debug state. This signal is rarely implemented as a pin on the target ASIC.

If DBGACK is available, the trace port analyzer's "Trigger Out" SMB port signal can be used to tell other test instruments when the microprocessor has stopped executing program code.

ASIC Design Guidelines

ASIC Pad Selection and Placement

The position and type of pad selected is based on the following factors:

- Minimizing noise and coupling between trace and other signals.
- Ability to drive the external load.

It has been shown that the quality of the TRACECLK signal, as observed by the trace port analyzer, has the greatest effect on the reliability of the system. This is because it is vital that TRACECLK transition move cleanly through the threshold region of the input circuitry of the trace port analyzer, without glitches or ringing.

It has been observed that with certain types of package and pin placement the signal coupling between the trace data signals and the trace clock can be significant. If this is observed to be a problem during simulations, it is recommended that GND or static I/O signals are placed on both sides of the TRACECLK signal.

Contact ARM for other ASIC design considerations.

Printed-Circuit Board Design Guidelines

Two cases need to be considered:

- A dedicated trace port. The trace port analyzer is the only load on the trace port signals.
- A shared trace port. The trace pins are shared with other functions; therefore, there are stubs on the printed-circuit board tracks of the development board, and there is an increased load on the output driver.

Dedicated Trace Port

This is the preferred way to connect a trace port analyzer to a trace port. With the trace port analyzer being the only load on the nodes connected to target ASIC pins, the main concern is signal integrity at the trace port analyzer connector. If you know the characteristics of your printed-circuit board tracks, use the actual trace impedance and propagation delay.

If you do not have access to this information, a rough rule of thumb for microstrip (trace on outer layer over a ground plane) on FR4 printed-circuit board is a propagation speed of 63 ps/cm (160 ps/inch). The impedance of a 0.127 mm (0.005) inch wide trace as a microstrip is from 70 to 75 Ω on a typical six-layer foil construction board. The impedance of a trace goes down as the width of the trace increases.

Knowledge of the characteristic impedance and signal edge rates of the Embedded Trace Macrocell (ETM) output drivers is necessary for proper design of the target system. Also required is the actual setup and hold provided by the ASIC ETM outputs with reference to the ETM TRACECLK. If you do not know the characteristics of the signals from your ASIC, consult your ASIC vendor. The variation between ASIC vendors on ETM output drivers and timing make it difficult to provide any general rule.

Printed-Circuit Board Track Length

Match all TRACECLK, PIPESTAT[2:0], TRACESYNC, and TRACEPKT[15:0] track lengths between the ASIC and the trace port connector within 100 ps. Overall differences of greater than 100 ps in track lengths directly impact setup and hold requirements. If the clock is delayed compared to the data, the setup specification needs to be increased by the additional clock delay. If any data is delayed compared to the clock, the additional delay needs to be added to the setup requirement. If data paths are such that data has both greater than and less than delays compared with the clock, the difference needs to be added to both the setup and hold specification.

Signal Quality

Reflections, overshoot, and undershoot all need to be minimized to ensure accurate data acquisition. The primary variable is the rise time of a signal compared to its track length. This is where the minimum signal rise and fall time becomes important.

The following points should be considered:

1. Ensure the one way propagation time for all tracks is less than 1/3 of signal rise time.
2. If tracks must be longer than 1/3 of the signal rise time, then some form of signal termination is required. The recommended method is series termination. The series resistor must be placed as close as possible to the ASIC pin. The value of this series resistor, when added to the output impedance of the signal driver should closely match the impedance of the printed-circuit board track.
3. If series termination cannot be used, add parallel or matched AC termination on each signal track at the trace port analyzer target header. This requires significantly more power from the ASIC, however, and the AC termination needs to closely match the frequency and rise time of the terminated signal. In practice, therefore, parallel termination will rarely be possible.
4. If the total track length is one rise time propagation delay or longer in length, follow standard high-speed design practices to minimize cross talk between the clock and the data signals.

Be aware that as the fabrication process for your ASIC improves, your output driver will probably improve and your rise and fall times decrease. If you are close to violating the requirements of point 1, consider adding termination to the signals to ensure continued correct operation.

NOTE: Note that ASIC output pads that have an output impedance that is matched to the printed-circuit board track may be available from your ASIC vendor. If these can be used, the signal quality of the trace port signals will be significantly improved.

Shared Trace Port

Some applications do not have enough pins available for trace; therefore, it may be necessary to multiplex trace signals with other functions. This has the effect of increasing the load on the trace signals, unless a specific trace-only development board can be built.

When an Embedded Trace Macrocell (ETM) output pin is multiplexed with other functions, the addition of the trace port analyzer target header can add a stub to the printed-circuit board track on the target system. To minimize the effect of the trace port analyzer target header on non-trace port analyzer based signal usage and still ensure the integrity of the trace measurements, apply the following constraints to design of the printed circuit board.

When the signal does not require termination in normal operation or is parallel terminated (this means that a full voltage swing signal travels down the track). Ensure that the propagation delay of the stub added for the trace port analyzer target header is 1/5 or less of the overall rise/fall time of the signal.

When the signal is series-terminated for normal operation (this means that a 1/2 voltage swing signal begins each transition on the track and propagates down the track until it is terminated at the target node). This case is full of potential problems. The 1/2 voltage swing signal can maintain the trace port analyzer input at its threshold voltage for longer than the required rise/fall time. You must move the trace port analyzer target header to within 1/5 rise time of the target end of the track to prevent this. If this is not possible, you must slow down the rise and fall times until this requirement can be met.

Header Connector Requirements

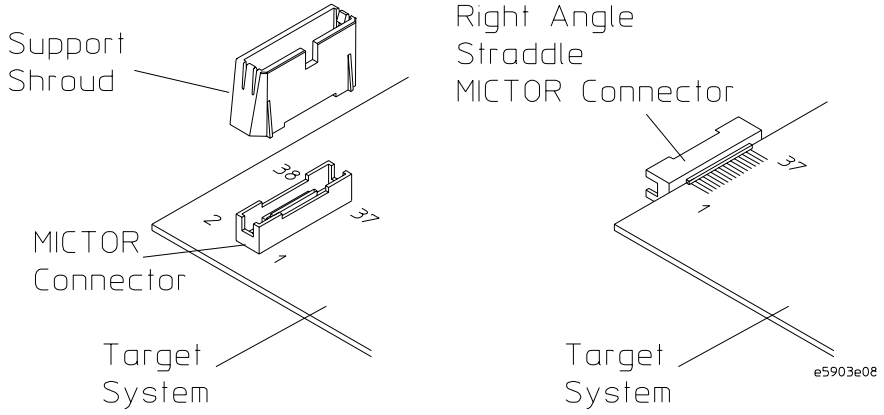
The target header is an AMP MICTOR Connector (0.64mm [0.025in]) pitch. The header has 38 pins and is organized such that it can handle:

- up to 16 trace data pins
- 3 pipeline status pins
- 1 trace sync pin
- 1 trace clock pin
- 1 external trigger pin
- 1 voltage reference pin
- 1 voltage supply pin (not used by the trace port analyzer)
- 9 JTAG run control pins

Recommended Orientation

The recommended ARM Embedded Trace Macrocell trace port connector orientation is displayed in the following diagram.

Connector Orientation



There are two choices for the target header: a vertical connector, and a right angle straddle mount connector.

NOTE: The vertical connector is recommended because it can accommodate an optional support shroud that provides additional strain relief and thus greater reliability. The notch on the support shroud should be placed on the same side as the odd numbered pins on the MICTOR connector. The support shroud is highly recommended.

The straddle mount connector should be used when board real estate is at a premium and there is no room for the vertical connector. A support shroud is not available for use with the straddle mount connector.

Connector and Support Shroud Part Numbers

The AMP part numbers for the MICTOR target headers are given below. These connectors may be purchased directly from AMP. Support shrouds and kits of five MICTOR connectors and support shrouds may be purchased from Agilent.

AMP MICTOR Headers Available from AMP

AMP Part Number	Description
2-767004-2	Vertical surface mount connector Ground bus lead length 1.397 mm (0.055")
767054-1	Vertical surface mount connector Ground bus lead length 2.743 mm (0.108")
767061-1	Vertical surface mount connector Ground bus lead length 3.505 mm (0.138")
767044-1	Horizontal straddle mount connector

Support Shrouds Available from Agilent

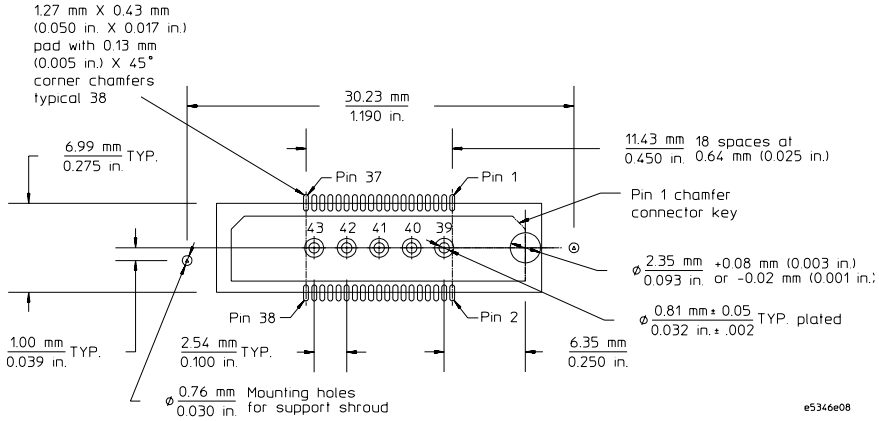
Agilent Part Number	Description
E5346-44701	Vertical support shroud for PCB thickness up to 1.575 mm (0.062")
E5346-44704	Vertical support shroud for PCB thickness from 1.575 mm (0.062") to 3.175 mm (0.125")
E5346-44703	Vertical support shroud for PCB thickness from 3.175 mm (0.125") to 17.780 mm (0.70")

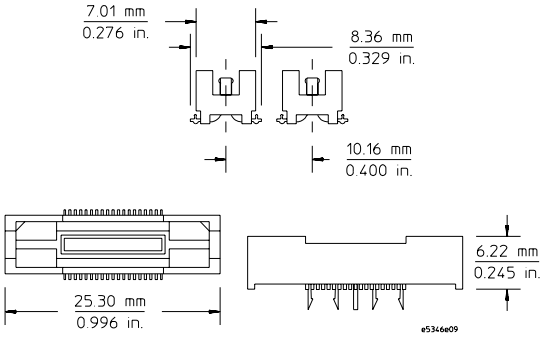
Set of Five MICTOR Connectors and Five Support Shrouds Available from Agilent

Agilent Part Number	Description
E5346-68701	Set of 5 MICTOR connectors and shrouds For PCB thickness up to 1.575 mm (0.062")
E5346-68700	Set of 5 MICTOR connectors and shrouds For PCB thickness from 1.575 mm (0.062") to 3.175 mm (0.125")

Connector Dimensions

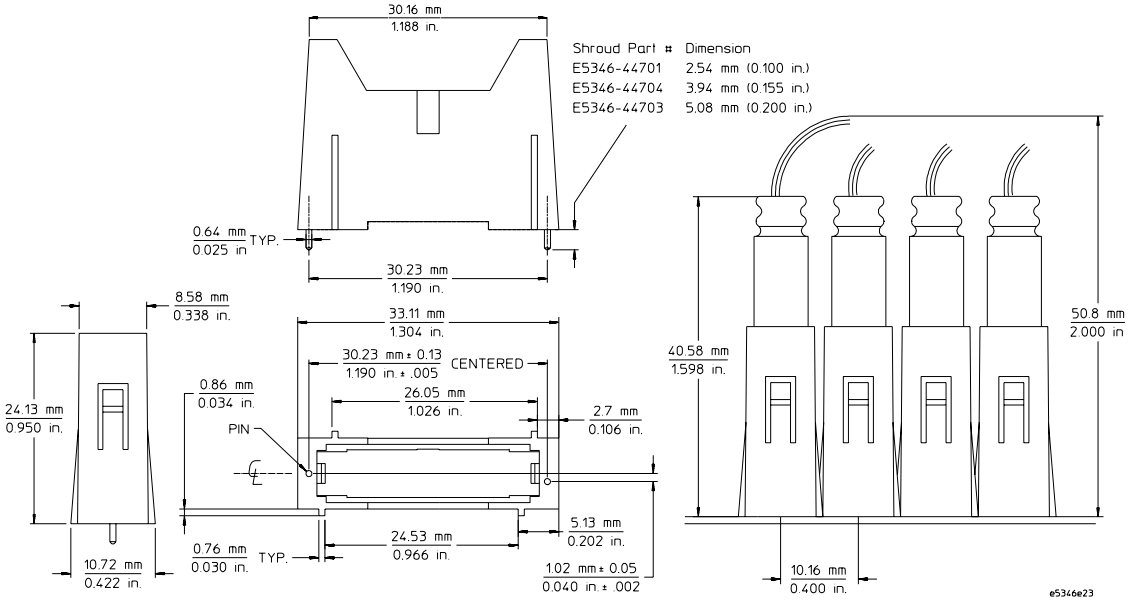
AMP MICTOR Connector Dimensions (AMP part # 2-767004-2)





Support Shroud Dimensions

Support Shroud Dimensions



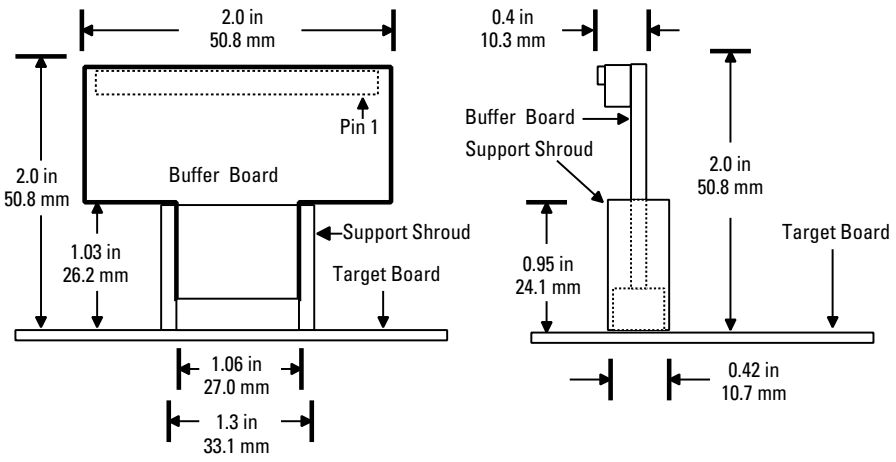
Height Restrictions and Keep-Out Requirements

The Agilent Technologies E5904B Option 300 trace port analyzer connects to the target MICTOR header with a small target probe (which is the 68-pin cable and a buffer board). The target probe connects either vertically or horizontally (right-angle), depending on which MICTOR header is on the target system.

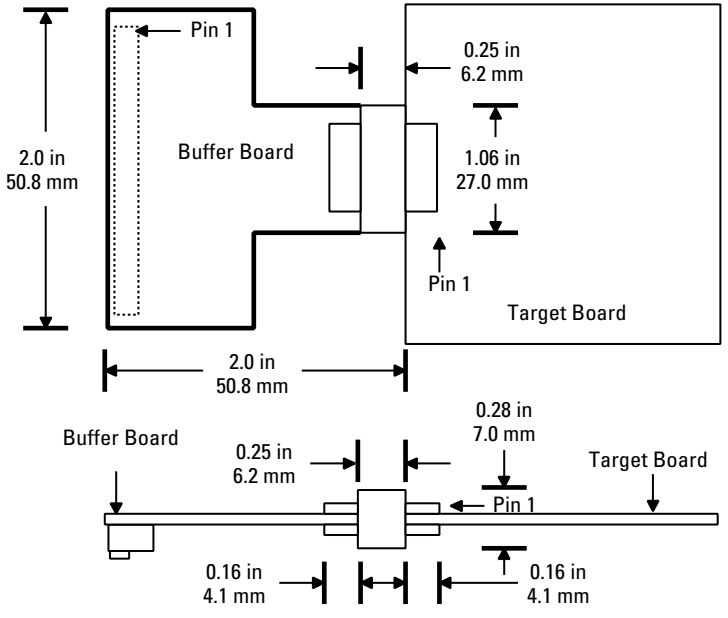
If the vertical header is used, make sure there is sufficient height clearance between the target system and the interface boards.

This section describes the height restrictions and keep-out for target probes using the single-processor ETM buffer board (E5903-66507) and for target probes using the dual-processor ETM buffer board (E5903-66508).

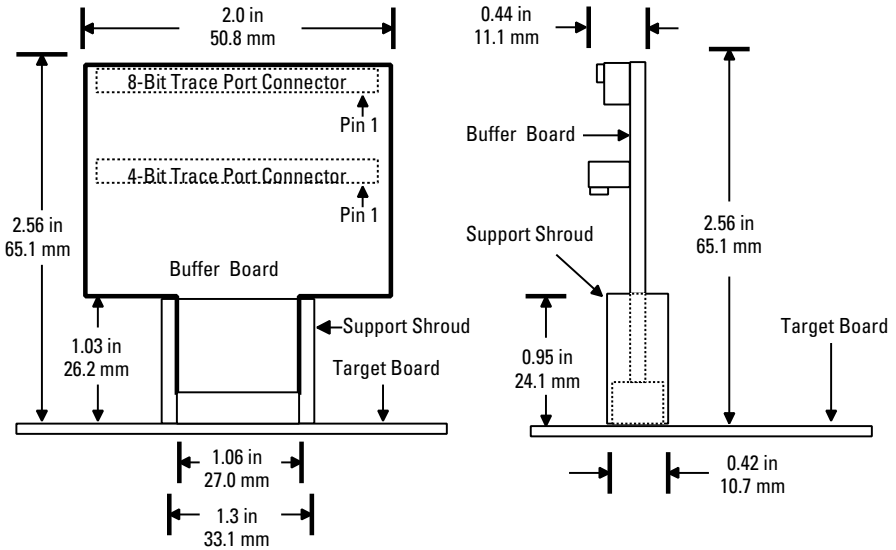
Single-Processor ETM Buffer Board (E5903-66507 or E5903-66516), Vertical Header, and Support Shroud



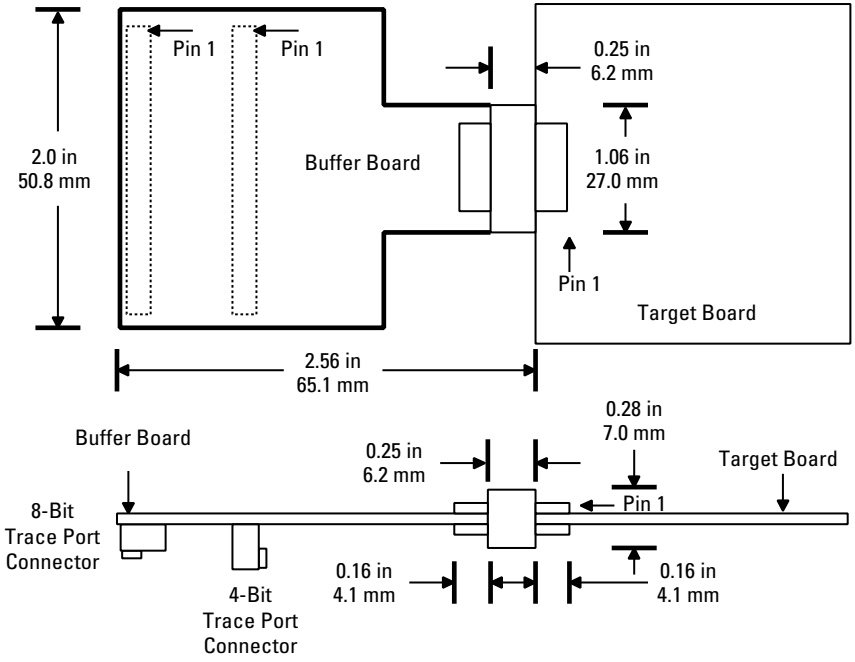
Single-Processor ETM Buffer Board (E5903-66507 or E5903-66516) and Right Angle Connector



Dual-Processor ETM Buffer Board (E5903-66508), Vertical Header, and Support Shroud



Dual-Processor ETM Buffer Board (E5903-66508) and Right Angle Connector



Connector Pin-Out

The Embedded Trace Macrocell (Rev 1) specification from ARM, release C or later, defines the following target header pin-outs. If your target system has these pin-outs, use the included trace port analyzer buffer board.

Single-Processor ETM Connector Pin-Out

The single-processor buffer board (E5903-66507) connects to the target system header connector on systems that use a single ARM processor.

Target Header Pin-Out for the MICTOR Connector, Single Processor ETM

Pin	Signal Name	Pin	Signal Name
38	PIPESTAT0	37	TRACEPKT8
36	PIPESTAT1	35	TRACEPKT9
34	PIPESTAT2	33	TRACEPKT10
32	TRACESYNC	31	TRACEPKT11
30	TRACEPKT0	29	TRACEPKT12
28	TRACEPKT1	27	TRACEPKT13
26	TRACEPKT2	25	TRACEPKT14
24	TRACEPKT3	23	TRACEPKT15
22	TRACEPKT4	21	nTRST
20	TRACEPKT5	19	TDI
18	TRACEPKT6	17	TMS
16	TRACEPKT7	15	TCK
14	VSupply	13	RTCK
12	VTref	11	TDO
10	EXTTRIG	9	nSRST
8	DBGACK	7	DBGRQ
6	TRACECLK	5	GND
4	No Connect	3	No Connect
2	No Connect	1	No Connect

NOTE: Pins 1, 2, 3, and 4 *must* be true no-connects. For designs with less than 16 trace data pins, pin 5 and any unused TRACEPKT pins *must* be connected to ground.

Dual-Processor ETM Connector Pin-Out

The dual-processor buffer board (E5903-66508) connects to the target system header connector on systems that use a two ARM processor cores.

Target Header Pin-Out for the MICTOR Connector, Dual Processor ETM

Pin	Signal Name	Pin	Signal Name
38	PIPESTAT_A0	37	PIPESTAT_B0
36	PIPESTAT_A1	35	PIPESTAT_B1
34	PIPESTAT_A2	33	PIPESTAT_B2
32	TRACESYNC_A	31	TRACESYNC_B
30	TRACEPKT_A0	29	TRACEPKT_B0
28	TRACEPKT_A1	27	TRACEPKT_B1
26	TRACEPKT_A2	25	TRACEPKT_B2
24	TRACEPKT_A3	23	TRACEPKT_B3
22	TRACEPKT_A4	21	nTRST
20	TRACEPKT_A5	19	TDI
18	TRACEPKT_A6	17	TMS
16	TRACEPKT_A7	15	TCK
14	VSupply	13	RTCK
12	VTref	11	TDO
10	EXTTRIG	9	nSRST
8	DBGACK	7	DBGRQ
6	TRACECLK_A	5	TRACECLK_B
4	No Connect	3	No Connect
2	No Connect	1	No Connect

NOTE: Pins 1, 2, 3, and 4 *must* be true no-connects. For designs with less than 16 trace data pins, unused TRACEPKT pins *must* be connected to ground.

Synchronous Trace Ports. The Agilent Technologies E5904B Option 300 trace port analyzer requires TRACECLK_A and TRACECLK_B even when the trace ports are synchronous. ARM recommends that you drive these two signals from two separate pins on your ASIC. (This has the advantage that you can run the trace ports asynchronously, without having to make changes to the printed-circuit board or the ASIC pinout.)

If it is not possible to use separate pins to drive TRACECLK_A and TRACECLK_B, you can drive both from the same pin. However, you must ensure that the ASIC pad driver is capable of driving the increased load and that the printed-circuit board track is series-terminated as close as possible to the pin of the ASIC.

Using the Trace Port Analyzer with ARM ETM revisions A or B

The Agilent E5904B Option 300 Trace Port Analyzer is designed for use with ARM ETM revision C or higher.

If you are using ARM ETM version A or B the MICTOR pinout will be different. You will need the Agilent E5903-66516 buffer board. Please send an e-mail requesting the E5903-66516 buffer board with your name and address to support_col@agilent.com, and one will be sent to you at no charge.

If you are unsure whether your target header pinout corresponds to ARM ETM revision A/B or revision C, compare your pinout to the following table.

Target Header MICTOR Connector Pin-Out for ARM ETM Revision A or B

Pin	ARM ETM Revision A or B	ARM ETM Revision C	Pin	ARM ETM Revision A or B	ARM ETM Revision C
38	PIPESTAT0	PIPESTAT0	37	TRACEPKT12	TRACEPKT8
36	PIPESTAT1	PIPESTAT1	35	TRACEPKT13	TRACEPKT9
34	PIPESTAT2	PIPESTAT2	33	TRACEPKT14	TRACEPKT10
32	TRACESYNC	TRACESYNC	31	TRACEPKT15	TRACEPKT11
30	TRACEPKT0	TRACEPKT0	29	VSupply	TRACEPKT12
28	TRACEPKT1	TRACEPKT1	27	VSupply	TRACEPKT13
26	TRACEPKT2	TRACEPKT2	25	EXTTRIG	TRACEPKT14
24	TRACEPKT3	TRACEPKT3	23	VTref	TRACEPKT15
22	TRACEPKT4	TRACEPKT4	21	nTRST	nTRST
20	TRACEPKT5	TRACEPKT5	19	TDI	TDI
18	TRACEPKT6	TRACEPKT6	17	TMS	TMS
16	TRACEPKT7	TRACEPKT7	15	TCK	TCK
14	TRACEPKT8	VSupply	13	RTCK	RTCK
12	TRACEPKT9	VTref	11	TDO	TDO
10	TRACEPKT10	EXTTRIG	9	nSRST	nSRST
8	TRACEPKT11	DBGACK	7	DBGRQ	DBGRQ
6	TRACECLK	TRACECLK	5	DBGACK	GND
4	No Connect	No Connect	3	No Connect	No Connect
2	No Connect	No Connect	1	No Connect	No Connect

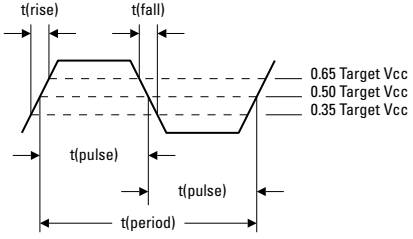
NOTE: Shaded areas indicate pin assignments that differ from ETM release C.

For further information contact Agilent Technologies or visit www.agilent.com/find/need-help

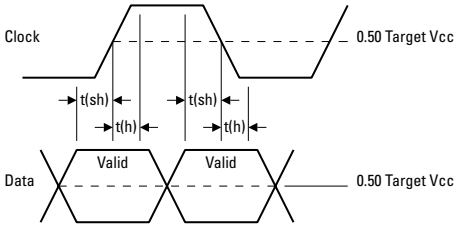
Timing and Voltage Specifications for Trace Port Signals

The signals from the target system must meet certain timing and voltage requirements in order for the Agilent Technologies E5904B Option 300 trace port analyzer to work correctly.

Signal Requirements



Clock Timing



Data Timing

Signal Requirements	
Maximum state clock frequency, single edge (single clock mode) t(period) = 1/frequency	200 MHz (1.65 Volts to 3.6 Volts Target VTref) 5 ns
Maximum state clock frequency, both edges (half clock mode) t(period) = 1/frequency	120 MHz (1.65 Volts to 3.6 Volts Target VTref) 8.3 ns
Minimum clock pulse width, t(pulse)	2 ns (see note 1)
Maximum clock/data rise and fall time, t(rise) and t(fall)	3.6 ns (see note 1)
Minimum clock/data rise and fall time	See PCB guidelines
Data setup/hold times, t(su)/t(h)	1.5/1.0 ns (see notes 2 and 3)

NOTES:
1. Clock/data rise and fall times are measured between 35% and 65% of Target VTref or ± 30% of programmed threshold.
2. Setup/hold is measured at Target VTref/2 or at programmed threshold.
3. For "both edge" clocking, setup/hold must be met for both rising and falling edge of clock.

Buffer Board—Required Voltage Levels

Absolute Maximum Ratings	Minimum	Maximum
Target VTref	-0.5 V	4.6 V [1]
Clock and Data	-0.5 V	4.6 V [1]
Input Current (Input < -0.05 V)		-50 mA

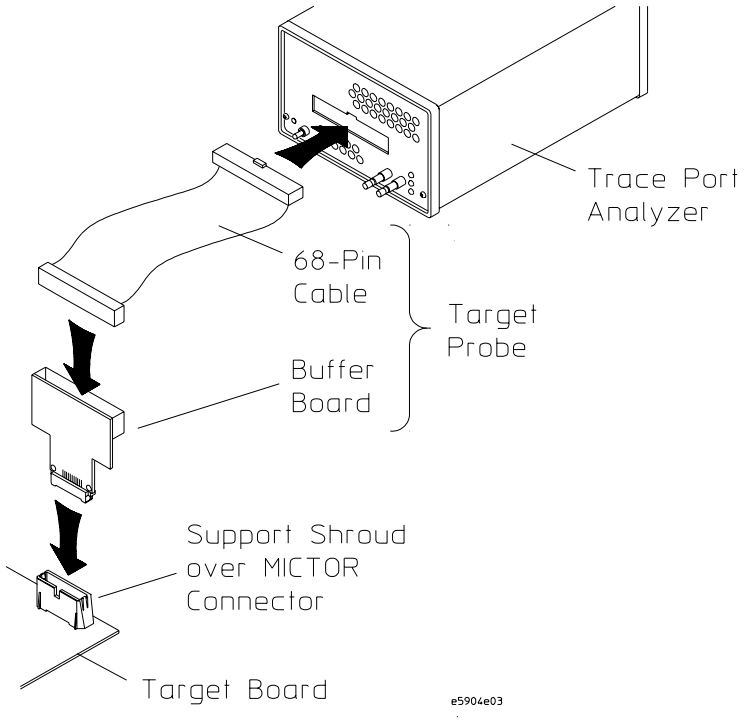
[1] Minimum voltage can be exceeded if maximum current rating is observed.

Recommended Operating Range	Minimum	Maximum
Target VTref	1.65 V	3.6 V
Clock and Data	0.0 V	3.6 V

DC Electrical Characteristics	Minimum	Maximum
Target VTref range	1.65 V	3.6 V
V_{ih}	0.65 VTref	
V_{il}		0.35 VTref

Loading Effects

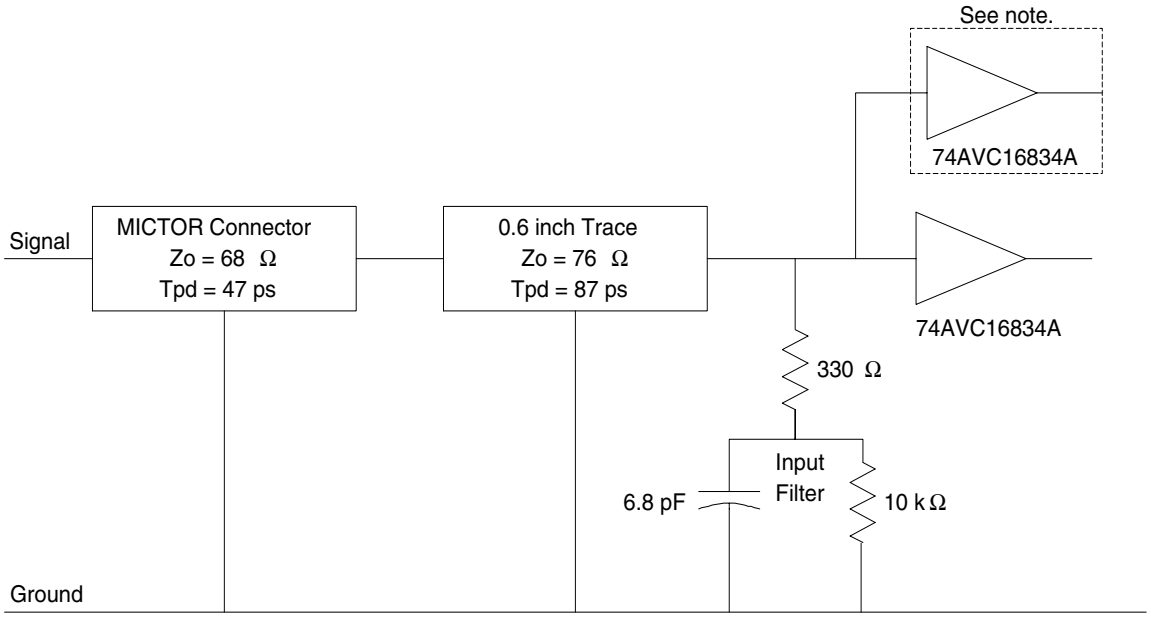
The trace port analyzer connects to the target system via the target probe as shown below:



Target Probe Equivalent Load

The trace port analyzer presents the following equivalent load to each signal. Target systems must be capable of driving this load and meeting the signal requirements given on page 38.

Trace Port Analyzer Buffer—Equivalent Load Model



NOTE: When using the E5903-66507 or E5903-66516 buffer board, TRACECLK drives an additional gate. TRACECLK drives only one gate when using the E5903-66508 buffer board. See page 5 for buffer board part numbers and descriptions.

Trace port analyzer probe characteristics (including target probe)	
Input resistance (DC)	10 kΩ ± 5%
Input capacitance, data inputs	4.0 pF
Input capacitance, clock input	6.5 pF
Maximum input voltage (all inputs)	3.6 Volts

Modeling the Trace Port Analyzer Buffer Board

The following characteristics can be used to model the trace port analyzer buffer board.

MICTOR Connector

The MICTOR connector (right-angle plug to right-angle receptacle or right-angle plug to vertical receptacle) can be modeled as a transmission line with Z = 68 Ω and Tpd = 47 ps.

PC Board

- The trace port analyzer buffer board has the following characteristics:
  - trace width = 0.127 mm (0.005 inches)
  - trace thickness = 0.0178 mm (0.0007 inches)
  - microstrip trace for TS, ES, BS, D0, and TrcClk signals
  - distance from traces to ground plane = 0.178 mm (0.007 inches)
  - spacing between traces = 0.508 mm (0.020 inches)
  - ground plane thickness = 0.0356 mm (0.0014 inches)
  - trace length = 15.24 mm (0.6 inches)
  - Er = 4.8

or

- Zo = 76 Ω, Tpd = 87 ps

Input Filter

In place of the buffer board characteristics, you can use discrete models of 330 Ω, 6.8 pF, and 10 kΩ as shown below.

Buffer IC

Use the IBIS model of a Philips 74AVC16834A IC in a TSSOP package. This model can be found on the Philips Semiconductor web site at:

http://www.philipslogic.com/support/ibis/avc/

The TRACECLK signal is connected to two inputs of the buffer IC on the E5903-66507 and the E5903-66516. TRACECLK drives only one gate when using the E5903-66508 buffer board. Data signals are only connected to one input of the buffer IC.

Undershoot/Overshoot

Undershoot must not go below -0.5 V at the input of the buffer IC. Overshoot must not go above 4.6 V at the input of the buffer IC.

Supporting JTAG-Only Debugging

There are special situations in which the target system designer may want to provide a separate run control (JTAG) header in addition to the MICTOR connector described in this document.

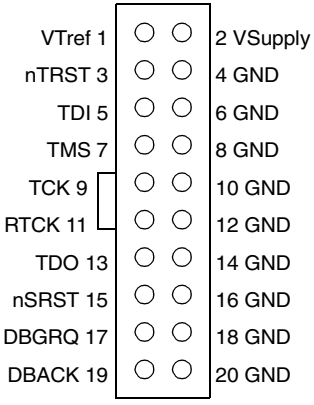
Including a Separate Run Control-Only (JTAG) Header

On a given design, some debug seats will use ARM ETM trace and JTAG run control. Other debug seats will use JTAG only.

Because the MICTOR connector is not compatible with most JTAG-only debug tools, the JTAG-only seats need some other way to connect to the target system.

In this case, the target board needs to provide a separate, run control-only (JTAG) header in addition to the MICTOR connector described in this document. This allows JTAG-only debug of the target board. The recommended header for the separate, JTAG-only connector is a medium-density 2 rows by 10 pins connector: 3M part number 2520-6002. JTAG signals may be routed to both the JTAG and MICTOR target headers; however, the two headers should be as close as possible to one another in order to avoid long signal paths and long stubs.

JTAG Run Control Connector Pin-Out



For complete information on designing a JTAG run control connector into your target system, see the document titled *Target Requirements for ARM Logic Analysis and ARM7TDMI/ARM9 Distributed Emulation Tools* on the web at:

http://www.tm.agilent.com/classes/MasterServlet?view=manual&man-ItemID=1000001216&language=eng&locale=US

2

Connecting to a Power Source

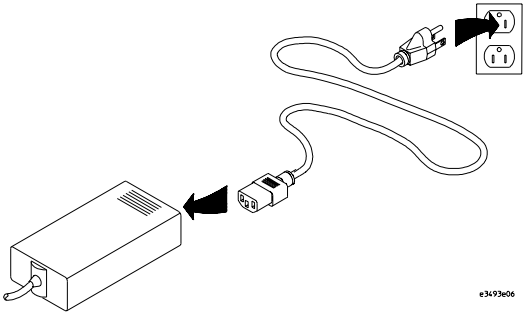
To connect the power supply

The trace port analyzer is shipped from the factory with a power supply and cord appropriate for your country. If the cord you received is not appropriate for your electrical power outlet type, contact your Agilent Technologies sales and service office (see "Contacting Agilent Technologies" on page 161).

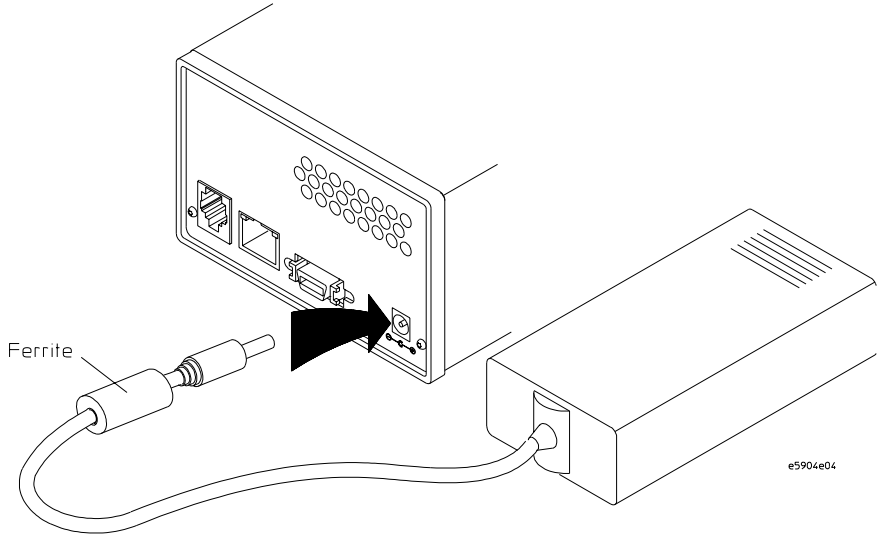
WARNING: Use only the supplied Agilent Technologies F1044B power supply and cord. Failure to use the proper power supply could result in electric shock.

CAUTION: Use only the supplied Agilent power supply and cord. Failure to use the proper power supply could result in equipment damage.

1. Install the ferrite on the 12 V power cord, near the end which plugs into the trace port analyzer.
2. Connect the power cord to the power supply and to a socket outlet.



3 Connect the 12 V power cord to the back of the trace port analyzer.

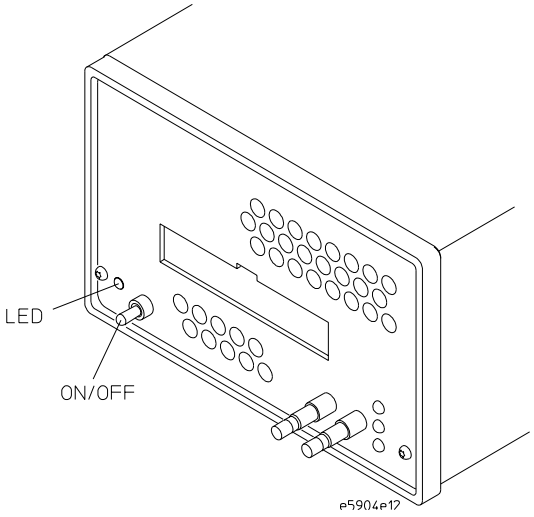


Ensure the power supply plug is completely seated in the power input receptacle.

To turn power ON

This procedure is for the trace port analyzer before it has been connected to a target system. (For the power ON procedure when connecting to a target system, see Chapter 6, “Connecting to a Target System,” on page 101.)

1 Turn ON the trace port analyzer power switch.



To turn power OFF

This procedure is for the trace port analyzer before it has been connected to a target system. (For the power OFF procedure when connected to a target system, see Chapter 6, “Connecting to a Target System,” on page 101.)

1 Turn OFF the trace port analyzer power switch.

3

Connecting to a LAN

Before a debugger can communicate with the trace port analyzer, the trace port analyzer must be connected to the LAN and set up with the proper LAN parameters.

The trace port analyzer has an IEEE 802.3 Type 10/100Base-TX LAN connector and is compatible with both 10 Mbps (10BASE-T) and 100 Mbps (100BASE-TX) twisted-pair ethernet LANs. (The trace port analyzer automatically negotiates the data rate for the LAN it is connected to.)

NOTE:

If the trace port analyzer is already active on the LAN and you wish to change its LAN parameters, you can use a "telnet" command on a networked computer to connect to the trace port analyzer; then, use the built-in "lan" command to change LAN parameters.

After making LAN parameter changes, you must cycle power to the trace port analyzer before the changes take effect. Doing this will break the network connection and end the telnet session.

Step 1. Decide on the LAN setup method

The trace port analyzer can be set up on the LAN (in other words, its LAN parameters can be configured) in two ways:

- By a DHCP (Dynamic Host Configuration Protocol) server that responds to BOOTP requests.
- By using a computer with terminal emulation software (or by using an actual terminal) connected to the trace port analyzer's serial (RS-232) port, and by entering commands to set the LAN parameters.

What is DHCP?

DHCP (Dynamic Host Configuration Protocol) allows clients (like the trace port analyzer) to obtain LAN parameters automatically from a server.

How does the trace port analyzer use DHCP?

The trace port analyzer uses "static allocation" (sometimes called "manual allocation") to obtain a permanent IP address. Every time the trace port analyzer is turned on, it sends out a BOOTP request packet. If the DHCP server on the network responds to BOOTP requests and has been configured to reply to the trace port analyzer's link-level address, it will respond with the IP address and other LAN parameters.

The trace port analyzer does not support "automatic allocation", which permanently allocates IP addresses from a pool of addresses.

Nor does the trace port analyzer support "dynamic allocation" of IP addresses—it does not track lease duration and request a new IP address when the lease is about to expire.

How does DHCP interact with other methods of setting LAN parameters?

Every time the trace port analyzer is turned ON, it sends out a BOOTP request packet (even if the LAN parameters have already been configured). As long as the DHCP server is configured to reply to BOOTP requests from the trace port analyzer's link-level address, it will respond with the IP address and other LAN parameters.

Step 2. Set the trace port analyzer's LAN parameters

- Find out whether port numbers 6470 and 6471 are already in use on your network and if that use constitutes a conflict.

  Computers on the network (running debugger software) communicate with the trace port analyzer through two TCP service ports. The default base port number is 6470. The second port has the next higher number (default 6471).

  In almost all cases, the default numbers (6470, 6471) can be used without change. If necessary, the base port number LAN parameter can be changed (using a serial port connection) if the port numbers conflict with some other product on your network.

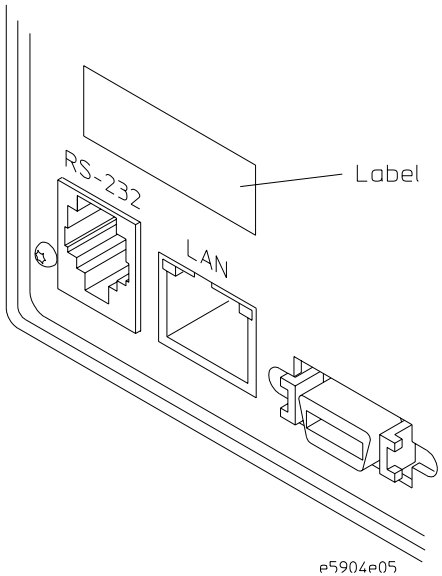
To set LAN parameters using DHCP

If there is a DHCP server on your network which responds to BOOTP requests and supports "static allocation" of IP addresses, it can be used to set the trace port analyzer's LAN parameters.

- Ask your system administrator to set up the IP address and other LAN parameters for the trace port analyzer on the DHCP server.

  You will need to supply the link-level address of the trace port analyzer.

  The link-level address (LLA) is printed on a label above the LAN connector on the trace port analyzer. This address is configured in each trace port analyzer shipped from the factory and cannot be changed.



To set LAN parameters using a serial port connection

The Agilent Technologies E5904B Option 300 trace port analyzer has a 9600 baud RS-232 serial interface with an RJ12 connector.

The trace port analyzer is shipped with a serial cable (with RJ-12 connectors on both ends, with 6-wire straight-through connections) and an adapter (female RJ-12 to female 9-pin D subminiature). The adapter plugs into 9-pin serial ports found on most PCs.

Serial connections on a workstation

If you are using a UNIX® workstation as the host computer, you need to use a serial device file. If a serial device file does not already exist on your host, you need to create one. Once it exists, you need to ensure that it has the appropriate permissions so that you can access it. See the system documentation for your workstation for help with setting up a serial device.

Serial connections on a personal computer

Serial connections are supported on personal computers. (You must use hardware handshaking if you will use the serial connection for anything other than setting LAN parameters.)

If you are using a personal computer as the host computer, you do not need to set up any special files.

1 Get the following information from your local network administrator or system administrator:

- An IP address for the trace port analyzer.

  You can also use a "LAN name" or "hostname" for the trace port analyzer, but you must configure it using the integer dot notation (such as 127.0.0.1).

- The gateway address.

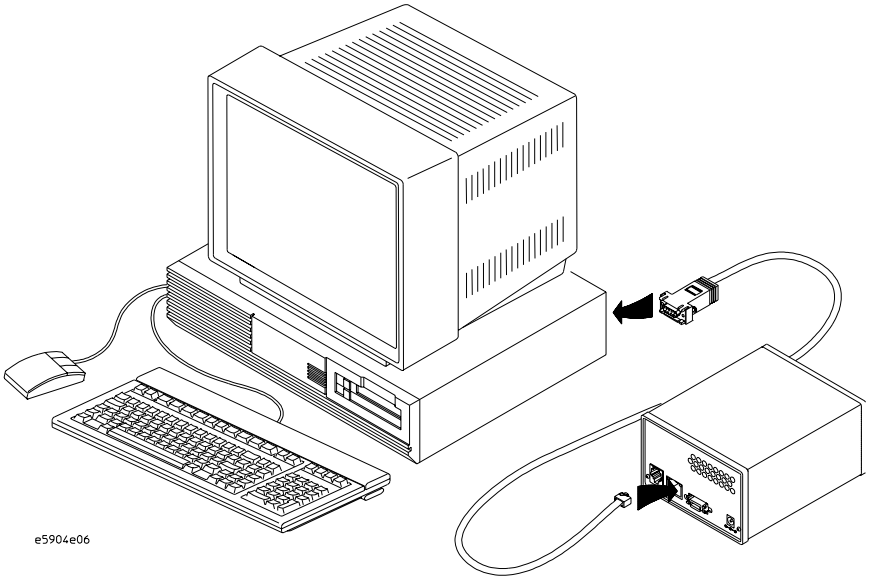
  The gateway address is an IP address and is entered in integer dot notation. The default gateway address is 0.0.0.0, which allows connections only on the local network or subnet. If connections are to be made to workstations on other networks or subnets, this address must be set to the address of the gateway machine.

- The subnet mask.

  A subnet mask blocks out part of an IP address so that the networking software can determine whether the destination host is on a local or remote network. It is usually represented as decimal numbers separated by periods; for example, 255.255.248.0.

2 Connect the serial cable from the host computer to the trace port analyzer.

Use the DB9-to-RJ12 adapter and the serial cable supplied with the trace port analyzer.



3 Start a terminal emulator program on the host computer.

If you are using a personal computer, the HyperTerminal application in Microsoft Windows® will work fine.

If you are using a UNIX workstation, you can use a terminal emulator such as cu or kermit.

4 Configure the terminal emulator program for:

- Communication rate: 9600 baud
- Data bits: 8
- Parity: none
- Stop bits: 1
- Flow control: none

5 Turn on power to the trace port analyzer.

When the trace port analyzer powers up, it sends a version message to the serial port, followed by a prompt.

6 Press the Return or Enter key a few times.

You should see a prompt such as "p>" or "R>".

If you don't see a prompt, refer to "If there are serial port connection problems".

For information about the commands you can use, enter "?" or "help" at the prompt.

7 Display the current LAN parameter settings by entering the **`lan`** command:

```
R>lan
lan is enabled
   Link Status is UP
   100BaseTX
  lan -i 15.5.24.116
  lan -g 15.5.23.1
  lan -s 255.255.248.0
  lan -p 6470
  Ethernet Address : 08000909BAC1
R>
```

The Ethernet address, also known as the link level address, is preassigned at the factory, and is printed on a label on the trace port analyzer.

8 Change the LAN parameters by entering **`lan`** commands using the following syntax:

```
lan -i <internet> [-g <gateway>] [-p <port>] [-s
<subnet>]
```

The lan command parameters are:

`-i <internet>` The IP address which you obtained from your network administrator.

`-g <gateway>` The gateway address. Setting the gateway address allows access outside your local network or subnet.

`-s <subnet>` This changes the subnet mask.

`-p <port>` This changes the base TCP service port number, normally 6470.

Do not change the default port numbers (6470, 6471) unless they conflict with some other product on your network. The numbers must be greater than 1024. If you change the base port, enter the new value in the configuration of your debugger (and, for UNIX workstations, in the /etc/services file).

Example

To assign an IP address of 192.6.94.2 to the trace port analyzer, enter the following command:

```
R>lan -i 192.6.94.2
```

If there are serial port connection problems

If the trace port analyzer prompt does not appear in the terminal emulator window (or terminal display) after pressing the Return or Enter key:

❏ Make sure that you have connected the trace port analyzer to the proper power source and that the power switch is on.

With certain serial (RS-232) port interface cards, connecting to a serial port when the trace port analyzer is turned off (or is not connected) will hang the personal computer. The only way to get control back is to reboot the computer. Therefore, we recommend that you always turn on the trace port analyzer before attempting to connect via a serial port.

❏ Make sure the serial cable is connected to the correct serial port on your computer (or terminal).

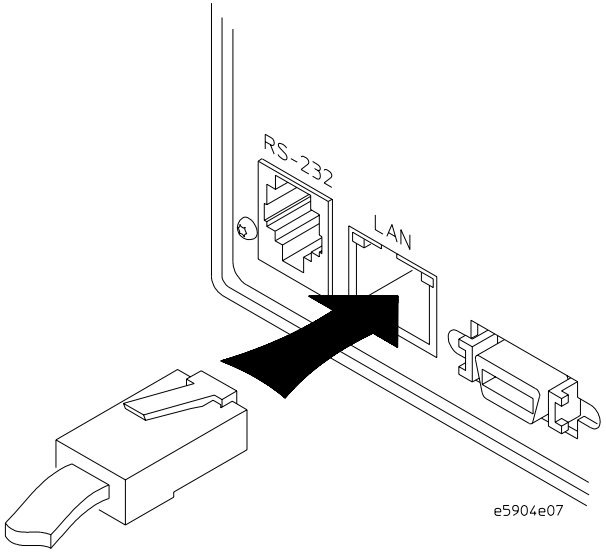
❏ Make sure you are using the serial cable and adapter which are supplied with the trace port analyzer.

❏ Make sure that you have properly configured the terminal emulator (or terminal) data communications settings:

- Communication rate: 9600 baud
- Data bits: 8
- Parity: none
- Stop bits: 1
- Flow control: none

Step 3. Connect the LAN cable

- Connect the LAN cable to the connector on the trace port analyzer.



Be sure to use the appropriate Category 3 or Category 5 cable for your LAN.

Step 4. Cycle power on the trace port analyzer

1 Cycle power on the trace port analyzer by powering it off then on again.

When using DHCP, you must cycle power in order for the trace port analyzer to send out a DHCPDISCOVER packet so that its LAN parameter settings can be set automatically by a server.

When using a serial connection, you must cycle power in order for the trace port analyzer's LAN parameter changes to take effect.

2 Wait at least 20 seconds for the trace port analyzer to recognize the LAN.

3 To verify that the trace port analyzer is now active and on the network, follow the instructions in the "Communicating with the Trace Port Analyzer" chapter.

Step 4. Cycle power on the trace port analyzer

4

Entering Commands

After the trace port analyzer has been connected to the LAN, there are two things you must do before you can configure the trace port analyzer:

- You must establish communications to the trace port analyzer from a networked computer.
- You must learn how to enter commands using the trace port analyzer's built-in command interface.

Establishing Communications over the LAN

Once the trace port analyzer has been connected to the LAN, it can communicate with computers on the network.

To use debugger software

The Agilent Technologies E5904B Option 300 trace port analyzer can be used with several third-party debuggers.

Debuggers typically provide some way to enter commands in the trace port analyzer's built-in command interface.

- Refer to your debugger's documentation for information on accessing the trace port analyzer's built-in command interface.

If the debugger cannot communicate with the trace port analyzer

Some debuggers have an initialization file that needs to be properly defined before a debugger can connect to the trace port analyzer.

❏ Check that the debugger is using the correct IP address for the trace port analyzer.

Refer to your debugger manual for information on specifying the trace port analyzer's IP address.

❏ Telnet to the trace port analyzer from the same networked computer that runs the debugger software (see "To 'telnet' to the trace port analyzer").

If the telnet connection works, check that the debugger has the correct IP address for the trace port analyzer.

If the debugger uses the network *hostname* for the trace port analyzer

(which doesn't work) and the telnet command uses the network *IP address* (which does work), the problem could be with the name server or host table lookup mechanism. If this is the case, try using the trace port analyzer's IP address in the debugger.

If the telnet connection doesn't work, refer to "Verifying Trace Port Analyzer LAN Communications" in the "Solving Problems" chapter.

To "telnet" to the trace port analyzer

1 Verify your trace port analyzer is now active and on the network by issuing a telnet command from a networked computer to the trace port analyzer's IP address.

Example

```
$ telnet 192.35.12.6
R>
R>
```

If you do not see a prompt, press the Return or Enter key a few times.

This connection will give you access to the trace port analyzer's built-in command interface.

2 To enter a command, type it in at the built-in command interface prompt, and press the Return or Enter key.

For example, to view the LAN parameters, enter the "lan" command.

Example

```
R>lan
lan is enabled
   Link Status is UP
   10BaseT
  lan -i 130.29.66.134
  lan -g 130.29.64.1
  lan -s 255.255.248.0
  lan -p 6470
  Ethernet Address: 0030D300A10C
```

3 To exit from the telnet session, type Ctrl+D at the prompt.

If you cannot “telnet” to the trace port analyzer

- ❏ Refer to “Verifying Trace Port Analyzer LAN Communications” on page 142.

Using the Trace Port Analyzer's Built-In Commands

The trace port analyzer has a built-in command interface which you can use for configuring or troubleshooting the trace port analyzer.

You can access the built-in command interface via:

- A telnet (LAN) connection.
- A "debugger command" window in your debugger.
- A serial connection (as may have been used in "To set LAN parameters using a serial port connection" on page 56).

Command Prompts

The prompt indicates the status of the trace port analyzer:

U	Running user program
M	Running in debug mode
p	No target power
R	Emulation reset
r	Target reset
?	Unknown state
x	Run control disabled

Commonly Used Commands

Command	Description
b	Break—go into the background monitor state.
cf	Configuration—read or write configuration options.
help	Help—display online help for built-in commands
init	Initialize—**init -c** re-initializes everything in the trace port analyzer except for the LAN software.
lan	Configure LAN parameters.
m	Memory—read or write memory.
reg	Register—read or write a register.
mtest	Memory test—test target system memory.
r	Run—start running user code.
rep	Repeat—repeat a command or group of commands.
rst	Reset—reset the target processor.
s	Step—do a low-level single step.
tlist	Display data captured by the trace port analysis unit.
trun	Start the trace port analysis unit's measurement.
tstatus	Display whether the trace port analysis unit is "running" or "stopped".
tstop	Stop the trace port analysis unit's measurement.
ver	Version—display the product number and firmware version of the trace port analyzer.

Use **`? <command>`** (or **`help <command>`**) to show the command syntax and required parameters for each command. For example, enter **`? mtest`** to show syntax and required parameters for the memory test command.

Examples

To reset the trace port analyzer and break into the monitor, enter:

```
R>rst -m
```

To set register r0, and then view r0 to verify that it was set, enter:

```
M>reg r0=ffff
M>reg r0
  reg r0=0000ffff
```

To break execution and then step a single instruction, enter:

```
M>b
M>s
  PC=xxxxxxxx
M>
```

To determine what firmware version is installed in the trace port analyzer, enter:

```
M>ver
```

Online Help

Use **help *command_name*** to see the command syntax.

Example

To get help on the memory command, enter:

```
M>help m

  m - display or modify processor memory space

    m <addr>               - display memory at address
    m -d<size> <addr>      - display memory at address with display size
    m -a<size> <addr>      - display memory at address using access size
    m <addr>..<addr>       - display memory in specified address range
    m <addr>..             - display 128 byte block starting at address A
    m <addr>=<value>       - modify memory at address to <value>
    m -d<size> <addr>=<value>        - modify memory with display size
    m -a<size> <addr>=<value>        - modify memory using access size
    m <addr>=<value>,<value>         - modify memory to data sequence
    m <addr>..<addr>=<value>,<value> - fill range with repeating sequence

  NOTES: For display and access size descriptions see mo command
```

Note that some of commands listed in the help screens are generic commands and may not be available for your trace port analyzer.

5

Configuring the Trace Port Analyzer

After you have established communications between the trace port analyzer and networked computer (using debugger or telnet software) and learned how to enter commands, you must set the trace port analyzer's configuration options appropriately for the target system.

Save trace port analyzer configuration settings to a file so they can be used to re-configure the trace port analyzer at the beginning of each debugger session.

Using the Built-In "cf" Command

You can configure the trace port analyzer using the built-in "cf" and "tcf" commands.

1 Establish communications with the trace port analyzer over the LAN.

You can either telnet from a networked computer or you can use the debugger. For more information, refer to "Establishing Communications over the LAN" on page 67.

Debuggers typically provide some way to enter commands in the trace port analyzer's built-in command interface, or they provide a window for configuring the trace port analyzer.

Example

```
M>cf speed
  cf speed=12MHz
M>
```

2 Enter the built-in "**`cf`**" and "**`tcf`**" commands to view the current configuration settings.

Example

```
M>cf
  cf proc=Arm966ES
  cf reset=auto
  cf rrt=no
  cf breakin=rising
  cf trigout=monhigh
  cf dbgack=no
  cf dbgreq=no
  cf speed=391KHz
  cf endian=little
  cf cparea=0x00000020
  cf comms=off
  cf vref=external
  cf thresh=1/2
  cf fastjtag=no
  cf hotplug=no
  cf vcatch=0x00
  cf monitor=no

M> tcf
  tcf bytes_per_state=2
  tcf clock_mode=single
  tcf time_tags=yes
  tcf rc_disable=no
  tcf message=no
```

3 Enter the "help cf" or "help tcf" command to see a complete list of the configuration items that may be set.

Example

```
M>help cf

  cf - display or set emulation configuration

    cf                - display current settings for all config items
    cf <item>         - display current setting for specified <item>
    cf <item>=<value> - set new <value> for specified <item>
    cf <item> <item>=<value> <item> - set and display can be combined

  help cf <item>    - display long help for specified <item>

  --- VALID CONFIGURATION <item> NAMES ---
    proc     - Set type of target processor
    reset    - RESET actions
    rrt      - Set restriction to real time runs
    breakin  - Break in control
    trigout  - Trigger out control
    dbgack   - Toggle availability of DBGACK
    dbgreq   - Toggle availability of DBGREQ
    speed    - Set JTAG clock
    endian   - Specify big or little endian
    cparea   - RAM region used by cpreg command
    comms    - Enable/disable debug comms channel polling
    vref     - Voltage reference
    thresh   - Voltage threshold
    fastjtag - Enable/disable fast debug mode
    hotplug  - Enable/disable hot plugging capability
    vcatch   - Set/display vector catch register for debug trap
    monitor  - Enable/disable monitor mode

M>help tcf

bytes_per_state
    tcf bytes_per_state=1
        The tlist command will output 1 byte of data per state.
    tcf bytes_per_state=2 - (default)
        The tlist command will output 2 bytes of data per state.
    tcf bytes_per_state=3
        The tlist command will output 3 bytes of data per state.

  clock_mode
    tcf clock_mode=single - (default)
        Trace data is captured on the rising edge of the clock.
    tcf clock_mode=half
        Trace data is captured on the rising and falling edges of the clock.

  time_tags
    tcf time_tags=no - (default)
        Time tags will not be output in the trace listing.
    tcf time_tags=yes
        Time tags will be output in the trace listing.

  rc_disable
    tcf rc_disable=no - (default)
        Run control signals are enabled.
    tcf rc_disable=yes
        Run control signals are disabled.
  message
    tcf message=no - (default)
        No asynchronous message.
    tcf message=trigger
        Asynchronous message generated when the trace port triggers
    tcf message=complete
        Asynchronous message generated when the trace port completes
        the collection of trace data.
```

4 To see a more detailed description of any configuration item, use the command "help cf <item>" or "help tcf <item>".

Example

```
M>help cf rrt

  Set restriction to real time runs

    cf rrt=no - (default)

       This option does not restrict to real time and will break into
       background temporarily if needed.

    cf rrt=yes

       This option restrict runs to real time which causes any command
       that requires a break to the monitor to be rejected except 'rst',
       'b', 'r' or 's'.
```

5 Use the **`cf`** and **`tcf`** commands to change the configuration settings (see "Setting the Configuration Options" on page 79).

See Also

For information on other built-in commands, see "Using the Trace Port Analyzer's Built-In Commands" on page 70.

Setting the Configuration Options

The configuration items must be set appropriately for each target system.

To set the type of ARM processor

Processor	Built-in command
ARM7TDMI (default)	cf proc=Arm7TDMI
ARM7DI	cf proc=Arm7DI
ARM710T	cf proc=Arm710T
ARM720T	cf proc=Arm720T
ARM740T	cf proc=Arm740T
ARM9TDMI	cf proc=Arm9TDMI
ARM 920T	cf proc=Arm920T
ARM 922T	cf proc=Arm922T
ARM 925T	cf proc=Arm925T
ARM 940T	cf proc=Arm940T
ARM 946ES	cf proc=Arm946ES
ARM 966ES	cf proc=Arm966ES

To specify whether DBGACK and DBGRQ are available

The Agilent Technologies E5904B Option 300 trace port analyzer for ARM will make use of the DBGACK and DBGRQ signals if they are made available on the target system header connector.

The DBGACK signal allows the trace port analyzer to quickly detect entry or exit from debug mode. If the DBGACK signal is available, it can be used to drive the trace port analyzer's "TRIGGER OUT" SMB port which can tell other test instruments when the microprocessor has stopped executing program code.

If the DBGRQ signal is available, the trace port analyzer can use it to cause the microprocessor to enter debug mode after receiving a signal from another test instrument on the trace port analyzer's "Break In" SMB port. In this way, for example, a logic analyzer's triggering capability can be used as a way to set complex breakpoints.

To make use of these signals, the trace port analyzer must be configured correctly. The following cf commands allow the specification of whether each signal is connected or not.

Value	Trace Port Analyzer configured for	Built-in command
yes	The corresponding signal is connected and will be used by the trace port analyzer.	cf dbgack=yes cf dbgreq=yes
no	The corresponding signal is not connected and will not be used by the trace port analyzer. (Default)	cf dbgack=no cf dbgreq=no

See Also

"To configure the Trigger Out SMB port" on page 92.

"To configure the Break In SMB port" on page 93

To specify whether runs are restricted to real-time

Value	Trace Port Analyzer configured for	Built-in command
no	Allows commands which break to the monitor. Examples include commands which display memory or registers. These commands break to the monitor to access the target processor, then resume the user program. (Default)	cf rrt=no
yes	No commands are allowed which break to the monitor, except “break,” “reset,” “run,” or “step.” The processor must be explicitly stopped before these commands can be performed.	cf rrt=yes

If your debugger allows displaying or modifying memory or registers while the processor is running, you must set “rrt=no” in order to use this feature.

To specify the JTAG clock speed

The trace port analyzer must be configured to communicate at a rate that is compatible with your target system processor. The JTAG clock speed (on the TCK signal) is independent of processor clock speed. However, the JTAG clock speed can be configured to match the target processor's clock speed if desired, using the RTCK signal.

CAUTION: Changing the TCK speed from a value in kHz or MHz to rtck (or vice versa) will re-initialize all internal variables including those associated with breakpoints and jtagch.

Value	Built-in command
391K - 40M	cf speed=*value*
Target processor clock speed	cf speed=*rtck*

The speed value can be a number followed by either K, which indicates the value is in kHz; or M, which indicates the value is in MHz. The clock can be set to speeds in the range 391 kHz to 40 MHz. Not all values in this range are valid; if an invalid speed is entered, the next slower valid speed will be used.

To match the JTAG clock speed to the target system clock

When the JTAG clock speed is set to "Return Clock" (cf speed=rtck), the trace port analyzer JTAG clock will attempt to match the target processor's clock. For this to succeed, the RTCK must be present at the header on the target system.

Entering **`cf speed`** without a value will display the current JTAG clock speed.

Configuring the Debug Port for Maximum Performance

The performance of the trace port analyzer depends on the speed at which it communicates with the target system. Better performance is obtained with faster communication speeds.

When to decrease TCK speed. Trace port analyzers are configured at the factory with a default TCK speed. In most cases, this is equal to the maximum allowable speed as specified by the manufacturer.

Processor	Manufacturer Spec. Max TCK (MHz)	Trace Port Analyzer Factory Default TCK (MHz)	Trace Port Analyzer Max TCK (MHz)
ARM	Design dependent	10	40

The default speed is suitable for most applications. However, the default speed is only valid if:

1. The processor is running at its full rated speed.
2. Trace lengths from the processor to the JTAG connector are short (two inches or less).
3. There are no stubs on the JTAG signals.

In some cases you may need to lower the TCK speed in order for the trace port analyzer to communicate reliably with the target system:

- When the target systems has additional loads on the JTAG lines.
- When the target system does not quite meet the requirements (as described in Chapter 1, “Target System Design Considerations,” on page 15).
- When you issue a break command and get the message "Unable to break".

When to increase TCK speed. Some target systems will allow TCK speeds greater than the default. The real maximum speed for a given target system can be determined empirically by increasing the speed and observing whether the communication to the target is reliable.

NOTE: Speeds greater than the default are not officially supported by Agilent Technologies or the chip manufacturer.

To specify whether TDO is latched for faster JTAG clock speeds

An additional configuration item, "fastjtag", controls when TDO data is latched. When "fastjtag" is configured to "yes," the trace port analyzer does not comply with JTAG timing parameters; however, this allows communication with the target at greater clock speeds provided the target does not violate standard JTAG timing parameters. When "fastjtag" is set to "yes," the maximum clock speed is 40 MHz.

Value	Meaning	Supported clock speeds	Built-in command
yes	TDO is latched late to allow maximum target clock speed.	391 kHz - 40 MHz	cf fastjtag=yes
no	Complies with JTAG timing parameters.	391 kHz - 10 MHz	cf fastjtag=no

When "fastjtag" is set to "no," 10 MHz is the highest speed you should enter using the "cf speed" command. Entering a value greater than 10 MHz will probably result in communication errors between the trace port analyzer and the target system. Enter a speed of 10 MHz or less to restore communication between the trace port analyzer and the target.

See Also

“Configuring the Debug Port for Maximum Performance” on page 82.

To specify the endian mode of the target system

Because the ARM7/ARM9 processor is capable of being configured as either big-endian or little-endian, the trace port analyzer must be told which the target system uses.

Value	Trace Port Analyzer configured for	Built-in command
little	Little endian (Default)	cf endian=little
big	Big endian	cf endian=big

To specify the coprocessor register RAM address

Reading and writing coprocessor registers requires a small area of target system RAM. The content of this RAM is saved before the RAM is used and the original content is restored after it is used. The **`cparea`** configuration item specifies the starting address of an 80 byte block of target system memory that must be readable and writable by the trace port analyzer. The default address is 0x20.

Example

To start the cparea at address 0x40, enter:

```
cf cparea=0x40
```

To set up and access coprocessor information

The firmware supports the description and access of coprocessors for the ARM core. Use the following commands to describe coprocessors.

To describe coprocessors:

```
cpdesc -d <CP#> <type> <reg> <size> <nbit> <rdbits>
cpdesc -r <CP#> R <reg> <size> <read0> <read1>
cpdesc -r <CP#> W <reg> <size> <write0> <write1>
cpdesc -r <CP#> B <reg> <size> <read0> <read1> <write0>
<write1>
```

To display coprocessor registration:

```
cpreg [-r <read0>] <CP#> <reg>
```

To set the processor register:

```
cpreg -s [-w <write0>] <CP#> <reg> <value1> [<value2>]
```

To display the description for the specified coprocessor register:

```
cpdesc <CP#> -
```

Parameter	Description
<CP#>	The coprocessor number.
<type>	R, W, or B for read, write, or both.
<reg>	A single register number or range (eg: 1 or 3...6).
<size>	The size of register in bytes (hex).
<nbit>	Bit 22 in an LDC or SDC instruction.
<rdbits>	Bits 15..12 in an LDC or SDC instruction.
<read0>	Bits 7..0 in an MRC instruction.
<read1>	Bits 23..16 in an MRC instruction.
<write0>	Bits 7..0 in an MCR instruction.
<write1>	Bits 23..16 in an MCR instruction.

NOTE: Entering a “cpdesc” command for a register already specified will overwrite previous data.

Example

To setup a description of coprocessor 15 read-only register 0 (ID register) for the ARM720T, enter:

```
cpdesc -r 15 R 0 4 00 00
```

To read CP15 c0, enter:

```
cpreg 15 0
```

To enable/disable debug communications channel polling

Value	Meaning	Built-in command
off	Disables polling for the debug communications channel.	cf comms=off
on	Enables polling for the debug communications channel.	cf comms=on

The debug communications channel provides a way for a running target system to communicate with a debugger in real-time.

Generally, your debugger will set this item if it supports the debug communications channel, and you can ignore it.

For more information, refer to your debugger manual.

To display/set communications channel information

The following commands will be used by a debugger to setup and use the debug communication channel. You can ignore them.

Command	Action
comm -b	Binary data upload (max=128 values). Record format: The first 2 bytes indicate the record length in bytes. A termination record (0x00, 0x00) follows. Example output for 10 words: 0x0028 (Data for 10 4-byte words) 0x0000 (Termination record)
comm -c	Displays comms control register status. Example Output: control=0 Write and read registers are clear. control=1 Data written to the comms data read register. control=2 Data available in the comms data write register. control=3 Data available in both registers.
comm -d	Display comms data buffer (max=128 values) Example output: Count=2 xxxxxxxx xxxxxxxx
comm -m <*count*>, <*value0*>, <*value1*>...	Modify comms data read register.
comm -m <*count*>	Number of values to be entered (max=96).
comm -r	Clear the write buffer.
comm -v	Enables verbose messages for data in comms data buffer.
comm -v enable	Enables verbose messages for data in comms data buffer. (Same as comm -v.)
comm -v disable	Disables verbose messages for data in comms data buffer.
comm -w	Display the number of words in the comms write buffer

See Also

For more information on the debug communications channel, see the ARM7/ARM9 data sheet.

To specify the reset behavior

The reset configuration item controls what happens when a reset occurs.

Value	Trace Port Analyzer configured for	Built-in command
auto	A RESET will break into monitor and restore watchpoint registers only when watchpoint registers are being used. (Default)	cf reset=auto
tomon (break)	A RESET will break into monitor. Watchpoint registers will be restored. The processor will remain in monitor until another command causes it to exit.	cf reset=tomon
touser (continue)	A RESET will not break into monitor. Watchpoint registers will not be restored.	cf reset=touser
restart	A RESET will break into monitor. Watchpoint registers will be restored and the user program will begin running.	cf reset=restart

Note that these actions occur only when the RESET signal is not asserted. Using the built-in **`rst`** command asserts RESET continuously until another command causes RESET to be negated.

To set up the vector catch register (ARM920T/922T/925T/940T/946ES/966ES)

This configuration item sets and displays the vector catch register, which defines which conditions will cause the processor to enter debug mode.

Bit	Meaning	Built-in command
7	FRQ	`cf vcatch=`*value*
6	IRQ	
5		
4	D_Abort	
3	P_Abort	
2	SWI	
1	Undef	
0	Reset	

Example

To set the vector catch register for SWI and RESET, set it to binary 00000101:

```
cf vcatch=0x5
```

To configure the monitor mode (ARM946ES/966ES)

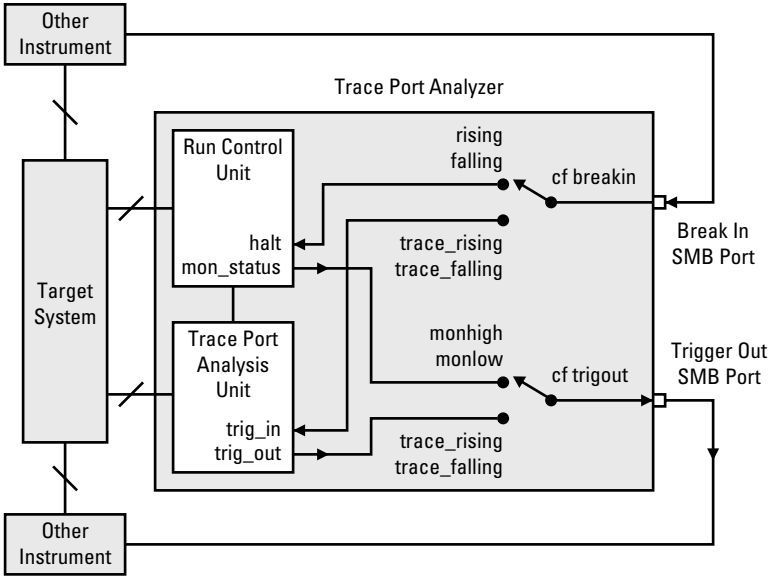
This configuration item controls the monitor mode bit in the debug control register.

Value	Meaning	Built-in command
no	Clears the monitor mode bit in the debug control register (Default).	cf monitor=no
yes	Sets the monitor mode bit in the debug control register.	cf monitor=yes

Generally, your debugger will set this item if it supports real-time debugging. For more information, refer to your debugger manual.

To configure the Trigger Out SMB port

Value	The Trigger Out SMB will	Built-in command
fixhigh	Always be high	cf trigout=fixhigh
fixlow	Always be low	cf trigout=fixlow
monhigh	Go high when the processor is running in background (Default)	cf trigout=monhigh
monlow	Go low when the processor is running in background	cf trigout=monlow
trace_high	Go high when the trace port trigger occurs.	cf trigout=trace_high
trace_low	Go low when the trace port trigger occurs.	cf trigout=trace_low



See Also "To specify whether DBGACK and DBGRQ are available" on page 80.

To configure the Break In SMB port

Value	The Break In SMB will	Built-in command
off	Inputs to the Break In SMB will be ignored.	cf breakin=off
rising	The trace port analyzer will cause a break on a rising edge. (Default)	cf breakin=rising
falling	The trace port analyzer will cause a break on a falling edge.	cf breakin=falling
trace_rising	A rising edge on the break in SMB port will cause a low-to-high transition on the EXTTRIG signal of the ETM connector.	cf breakin=trace_rising
trace_falling	A falling edge on the break in SMB port will cause a low-to-high transition on the EXTTRIG signal of the ETM connector.	cf breakin=trace_falling

See Also "To specify whether DBGACK and DBGRQ are available" on page 80.

To configure the voltage reference

The trace port analyzer normally uses the VTref signal on the JTAG connector to determine logic high and logic low levels when driving the TDI and TCK signals.

However, you can specify that the trace port analyzer use an internally generated voltage reference instead, when:

- The target system connector does not have the correct voltage on the VTref pin.
- You plan to use the hot plug-in procedure for connecting the trace port analyzer to the target system.
- You have some other non-standard situation.

Value	Meaning	Built-in command
external	The voltage reference is generated by the target system and is found on the Vref pin of the header connector. (Default)	cf vref=external
value	The voltage reference of *value* is generated internally by the trace port analyzer. The value is a number followed by either mV, which indicates the value is in millivolts, or V, which indicates the value is in volts.	cf vref=*value*

CAUTION: The cf vref=value option should only be used if the core voltage is different than that of the Vref signal on the JTAG connector or when the trace port analyzer is configured for hot plug-in. Use this option with extreme care, because it is possible to damage the target system if the voltage level is chosen incorrectly.

To specify the run control threshold voltage

Threshold for run control voltage reference. Voltages above (vref × thresh) will be considered logic high and voltages below this level will be considered logic low.

Value	Built-in command
1/2 (**Default**)	cf thresh=1/2
2/3	cf thresh=2/3
1/3	cf thresh=1/3

The threshold voltage for the trace port is fixed at 1/2 of the reference voltage.

To configure the trace port analyzer for hot plug-in

This configuration item allows the powered-on trace port analyzer to be connected to a powered-on, running target system without halting processor execution.

Value	Meaning	Built-in command
no	The probe works normally (Default).	cf hotplug=no
yes	The probe can be connected to a running target without causing the target to halt. Because the trace port analyzer cannot detect the voltage reference when it is not plugged into the target system, the **`cf vref=`*`target_voltage`*** command must be issued to reset the voltage reference after issuing the **`cf hotplug=yes`** command. The voltage reference must be set to the target voltage.	cf hotplug=yes

NOTE: The trace port analyzer speed must not be set to "rtck" when using hot plug-in because the processor clock signal that the trace port analyzer is attempting to match is only available when the JTAG port is connected.

Normally the nSRST line is held low, and connecting the JTAG connector to the target system causes the processor to reset. The cf hotplug configuration item holds the nSRST line at Vref when the trace port analyzer is hot plugged to the JTAG connector.

See Also

"To specify the JTAG clock speed" on page 82.

"Using the Hot Plug-in Procedure" on page 106.

To save and restore configuration option settings

NOTE: The configuration option settings on the preceding pages can be stored using the `cfsave -s` command. The configuration option settings that use the "tcf" commands on the following pages will not be saved with the `cfsave -s` command.

- Use the "cfsave -s" command to store all configuration option settings in the trace port analyzer's flash memory.
- Use the "cfsave -r" command to restore the most recently saved configuration option settings.

  If the trace port analyzer is re-initialized, it will return to all the default configuration option settings. You can use the "cfsave -r" command to restore the configuration option setting that were last saved.

To specify the amount of data per trace state

This configuration item tells the trace port analyzer how to present captured data to the debugger.

With a 4-bit trace port, 8 bits of data is output per trace clock when the PIPESTAT[2:0] and TRACESYNC data is included. Likewise, on each trace clock, 12 bits of data is output with an 8-bit trace port, and 20 bits of data is output with a 16-bit trace port.

Usually, the debugger will set this configuration item appropriately.

Value	Meaning	Built-in command
1	The tlist command will output 1 byte of data per state.	tcf bytes_per_state=1
2	The tlist command will output 2 bytes of data per state. (Default)	tcf bytes_per_state=2
3	The tlist command will output 3 bytes of data per state.	tcf bytes_per_state=3

To specify the clock mode

This configuration item tells the trace port analyzer about the target system's trace port clocking method.

The target system's trace port can be clocked on either the rising edge of the processor clock (single edge clock) or both the rising and falling edges of the processor clock (double edge clock).

Value	Meaning	Built-in command
single	Trace data is captured on the rising edge of the clock. (Default).	tcf clock_mode=single
half	Trace data is captured on the rising and falling edges of the clock.	tcf clock_mode=half

To specify use of time tags

This configuration item tells the trace port analyzer whether to add time tags to the trace listing. Time tags indicate the time of a particular state in the trace listing relative to the trigger. Time tags record the time that the trace data was received by the trace port analyzer, not the internal execution time of the processor.

Value	Meaning	Built-in command
no	Time tags will not be output in the trace listing.	tcf time_tags=no (default)
yes	Time tags will be output in the trace listing.	tcf time_tags=yes

To specify whether the trace port analyzer run control signals are disabled

Some users may want to use a probe other than the trace port analyzer for run control of the target system. The trace port analyzer's run control signals can be disabled to prevent signal contention between the trace port analyzer and the additional run control probe. This gives the additional probe run control over the target system.

CAUTION: To prevent equipment damage, the trace port analyzer run control signals must be disabled before connecting the additional probe.

Value	Meaning	Built-in command
no	Run control signals are enabled.	tcf rc_disable=no (default)
yes	Run control signals are disabled.	tcf rc_disable=yes

To specify when asynchronous messages are generated

The trace port analyzer can generate an asynchronous message when the trace port analyzer has been triggered or when the trace port buffer is full. This feature is provided for use by the debugger software.

Value	Meaning	Built-in command
no	No asynchronous messages are generated.	tcf message=no
trigger	An asynchronous message is generated when the trace port triggers.	tcf message=trigger
complete	An asynchronous message is generated when the trace port completes the collection of trace data.	tcf message=complete

6

Connecting to a Target System

After the trace port analyzer has been properly configured for the target system, you can connect it to the target system and verify its operation. You can plug the trace port analyzer into the target system using:

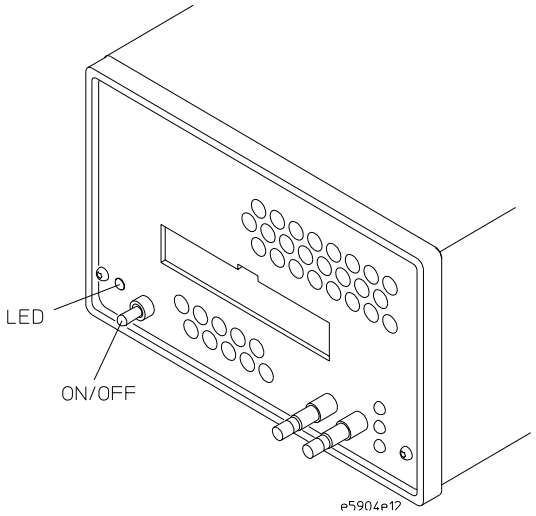
- The normal plug-in procedure.
- The hot plug-in procedure.

Using the Normal Plug-in Procedure

The normal plug-in procedure, with the trace port analyzer and the target system both powered OFF, involves the following steps.

Step 1. Turn OFF power to the target system.

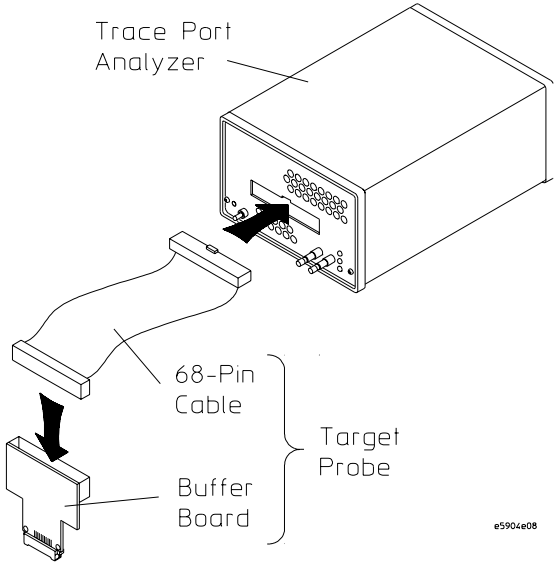
Step 2: Turn OFF the trace port analyzer power switch.



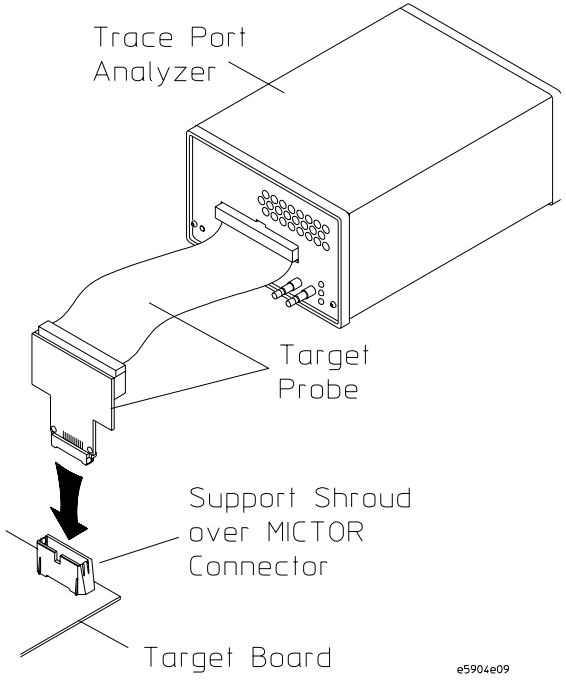
Step 3. Connect the trace port analyzer to the target probe

1 Plug one end of the 68-pin cable into the trace port analyzer.

2 Plug the other end of the 68-pin cable into the connector on the buffer board.



Step 4. Plug the target probe into the target system MICTOR header connector.



Step 5. Turn ON the trace port analyzer power switch.

Step 6. Turn ON power to the target system.

Using the Hot Plug-in Procedure

The hot plug-in procedure, with both the trace port analyzer and the target system both powered ON, involves the following steps.

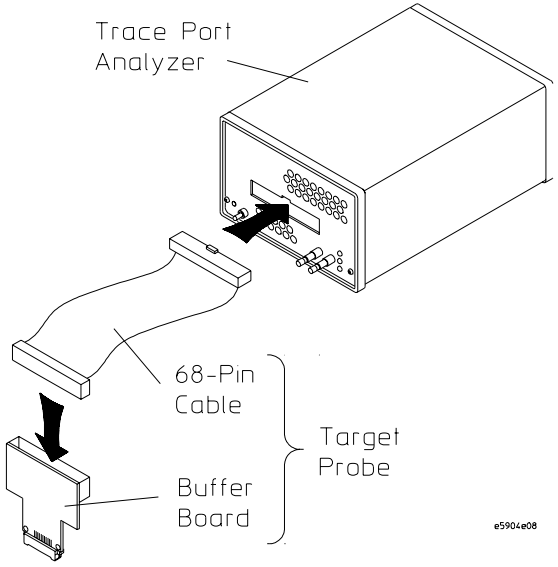
Step 1. Configure the trace port analyzer for hot plug-in

- See "To configure the trace port analyzer for hot plug-in" on page 96.

Step 2. Connect the trace port analyzer to the target probe

1 Plug one end of the 68-pin cable into the trace port analyzer.

2 Plug the other end of the 68-pin cable into the connector on the buffer board.



Step 3. Turn ON the trace port analyzer power switch if it is not already ON.

CAUTION: Under no circumstances should an powered-OFF trace port analyzer be connected to a powered-ON target system when performing the hotplug procedure.

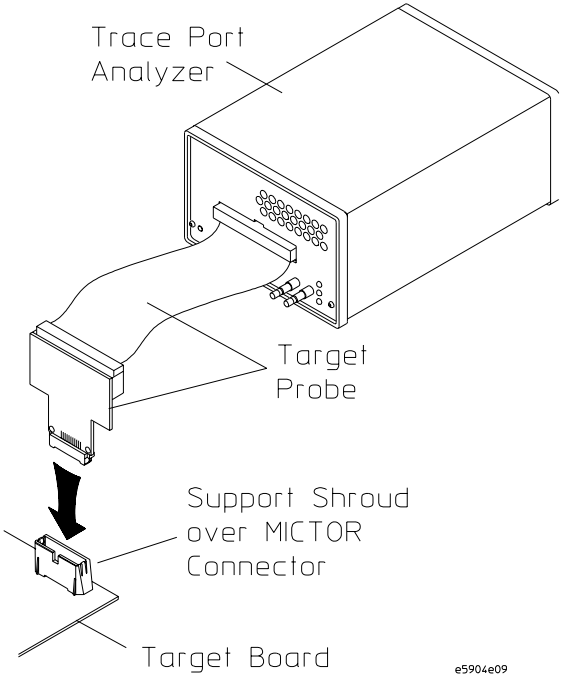
Step 4. Set trace port analyzer configuration

Be sure to set the following configuration items before connecting the trace port analyzer to the target system:

- Processor type (See page 79.)
- JTAG clock speed (See page 82.)
- Voltage reference (See page 94.)
- Hotplug (See page 96.)

You must set the configuration items before connecting the trace port analyzer to the target system to prevent unexpected system behavior. If this is not done, the target may go into reset when the trace port analyzer is connected, or other unexpected behavior may occur.

Step 5. Plug the target probe into the target system MICTOR header connector.



Verifying the Target System Connection

After the trace port analyzer has been plugged into the target system, you should verify that the trace port analyzer works correctly.

To verify trace port analyzer operation

❑ Perform some simple tests in the debugger to verify that the trace port analyzer is working properly with the target system.

If the trace port analyzer doesn't work with the debugger

Most problems are associated with not having the trace port analyzer and target system properly configured or initialized.

❑ Initialize the trace port analyzer and target system so that the debugger can connect.

Refer to your debugger manual for proper initialization.

If there are target system interaction problems

❑ See "Verifying Run Control Interaction with the Target System" on page 147.

7

Configuring for Multiple Processor Systems

The Agilent E5904B Option 300 trace port analyzer supports trace of multiple processors through a single JTAG scan chain. The trace port analyzer supports JTAG chain connections (TDO to TDI, not star) for up to 32 processors. The default configuration is for a single processor.

Known and Unknown Processors

In this chapter, “unknown” processor refers to processors in the JTAG scan chain which are not explicitly supported by the firmware (driver).

To configure the trace port analyzer for multiple processor trace

The jtagch command defines a list of processors for the JTAG scan chain. The firmware (driver) that has been loaded into the trace port analyzer supports a particular processor or a family of processors (e.g. ARM). The JTAG scan chain may contain processors both known and unknown by the trace port analyzer firmware.

Command Syntax

All processors must be specified in the JTAG scan chain (jtagch) list. The command syntax is as follows:

```
jtagch <driver link|IR length 1>,
       [driver link|IR length 2],
       [driver link|IR length 3]...
```

NOTE: Values enclosed in <angle brackets> are required, values enclosed in [square brackets] are optional. The "|" symbol indicates "or."

The first processor in the list is identified as processor 1, the next processor is identified as processor 2, etc. A maximum of 32 processors (known and unknown) can be specified in the jtagch command. The default setting is `jtagch a`.

Processors that are recognized by the emulation firmware are identified by `driver link`. Unknown processors are identified by `IR length`. Commas are used to separate processors in the jtagch list. The list of processors must contain at least one known processor.

The `driver link` is for the ARM family of processors is "`a`".

The `IR length` is the processor Instruction Register (IR) length in number of bits.

To display the current list of valid processors, issue the command `jtagch` with no parameters.

To direct a command to a specific processor

The sp command allows you to direct commands and data to and from a specific processor. Initially, if an `sp <processor identifier>` command has not been issued, commands will be sent to the first known processor in the JTAG scan chain. Once the sp command has been used to address a particular processor, that choice will not change until another `sp <processor identifier>` command is issued or a system initialization occurs. The syntax for the sp command is:

```
sp <processor identifier>
```

The <processor identifier> must be set for a known processor in the JTAG scan chain list.

The sp command without the <processor identifier> will display the current processor identifier.

Numbering of processors for the <processor identifier> term includes all known and unknown processors.

Examples

Given the JTAG scan chain:

jtagch a, a

To read the registers and memory location 100 in the first processor in the list, issue the command sequence:

```
sp 1
reg
m 100
```

To read the registers and look at the emulation status in the second processor, issue the command sequence:

```
sp 2
reg
es
```

Given the JTAG scan chain:

jtagch 9, a, a

To read the registers and memory location 100 in the second processor, issue the command sequence:

```
sp 2
reg
m 100
```

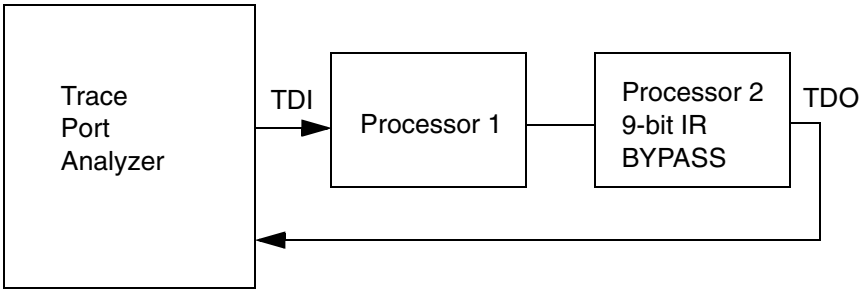
To direct a command to all known (non-bypassed) processors

Some commands can be issued to all know processors. These commands are:

`es all`	Display the emulation status of all known processors
`b all`	Break into all known processors
`r all`	Run all known processors

Multiple processor system example — one known processor and one unknown

Consider a system of two processors in a serial JTAG chain configuration with a single LAN connection to the trace port analyzer. The JTAG chain contains one known processor while the other is an unknown processor (e.g. a DSP) which has a 9-bit instruction register (IR).



To setup this JTAG connection use the following command:

```
jtagch a,9
```

The above jtagch command says that the first processor is known by a driver and it is linked to driver "a." The next processor (Processor 2) is not known and has an instruction register length of 9 bits.

When the proper JTAG scan chain is set up, the trace port analyzer can issue commands and access resources for Processor 1 while Processor 2 is always placed in a bypass mode. The trace port analyzer will issue the proper JTAG scan chains so that the commands and data will be directed only to Processor 1. The connection will look just like a single processor connection.

To enable Processor 1 breakpoint:

```
bc -e swbp
```

To set a breakpoint for Processor 1 at address 0x1000:

```
bp 1000
```

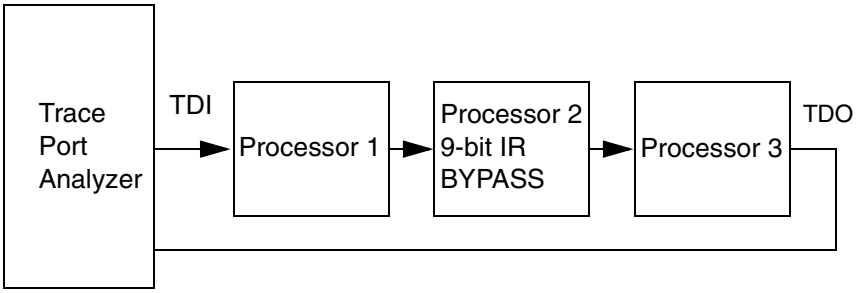
Whenever the processor hits a breakpoint the following message is

returned:

```
!ASYNC_STAT 615! Software breakpoint:  00001000
```

Multiple processor system example — two known processors, one unknown

Consider a system of two known processors and one unknown processor. The unknown processor has an IR length of 9 bits.



To setup this JTAG scan chain use the following command:

```
jtagch a,9,a
```

To issue commands to and receive data and messages from Processor 1 enter the command:

```
sp 1
```

then issue the desired commands.

To issue commands to and receive data and messages from Processor 3 enter the command:

```
sp 3
```

then issue the desired commands.

To enable Processor 1 breakpoints:

```
sp1
bc -e swbp
```

To set a breakpoint for Processor 1 at address 0x1000:

```
sp1
bp 1000
```

To set a breakpoint for Processor 3 at address 0x2000:

```
sp 3
bc -e swbp
bp 2000
```

When processor 1 hits a breakpoint the following message is returned:

```
!ASYNC_STAT 615! Software breakpoint:  00001000:
Processor 1
```

When processor 3 hits a breakpoint the following message is returned:

```
!ASYNC_STAT 615! Software breakpoint:  00002000:
Processor 3
```

NOTE: Other asynchronous messages will display the processor number at the end of the message only when there is more than one known processor in the JTAG scan chain.

8

Collecting Trace Data from a Multiple ARM Core ETM System

Getting Execution Trace from Multiple ARM Processors

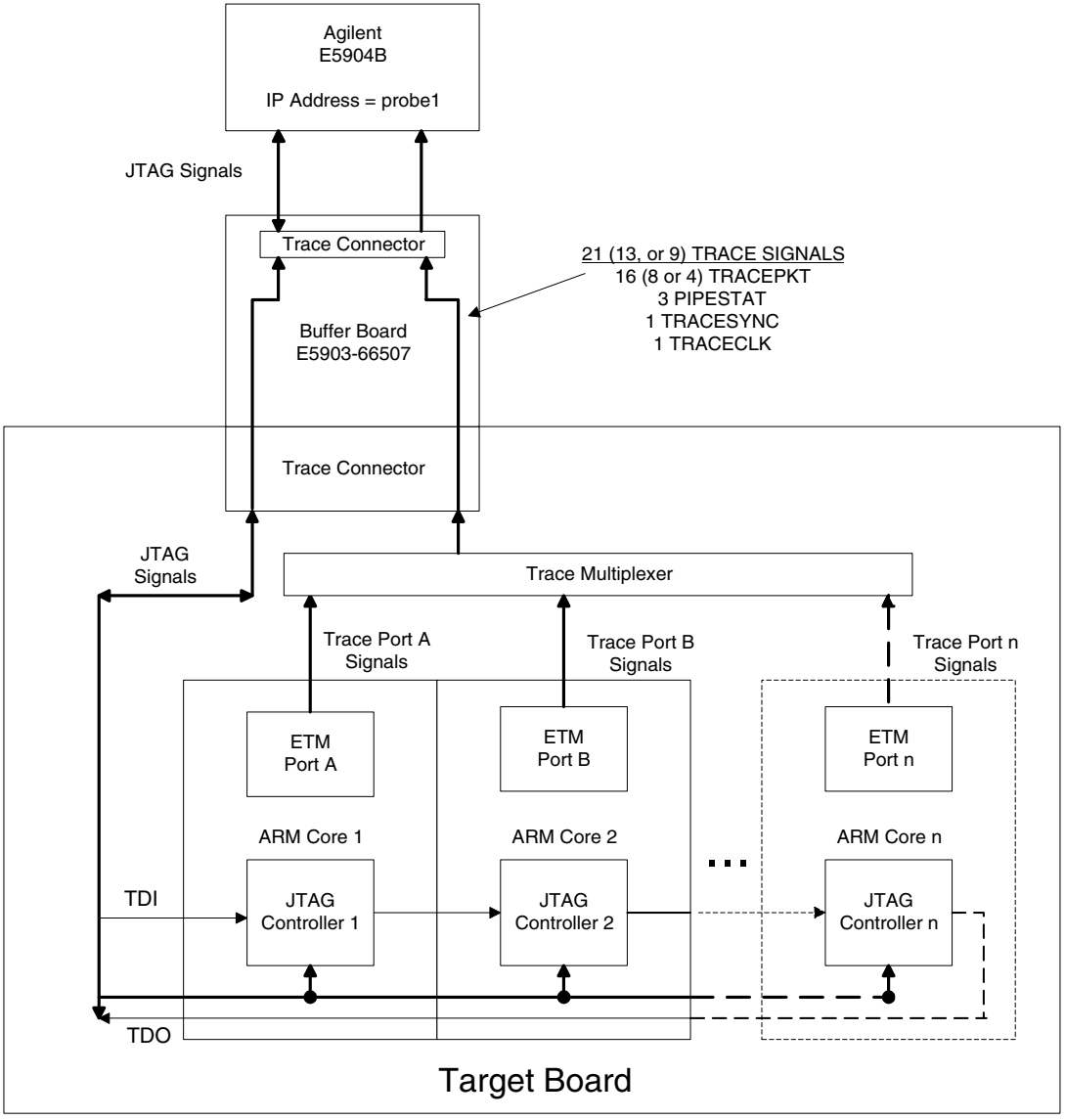
The following block diagrams show possible setups of a multiple ETM system with a trace multiplexer directing the signals to the trace connector. The trace multiplexer is implemented on the ASIC or Target board. It is not part of the trace port analyzer.

Collecting Full Trace from a Selected ETM in a Multiple Core System

This setup allows the user to control a multiple core system. The trace port analyzer provides run control for all cores, and provides trace capability for one full complement of trace port signals (up to 16 trace packet signals) from one ETM on the target system.

The signals that are routed to the trace port analyzer must be controlled by a trace multiplexer. It is up to the customer to design, implement, and control the trace multiplexer. The trace multiplexer will route the signals from the multiple ETMs on the target system to the trace port connector on the target board.

One trace port analyzer and a target probe (68-pin cable and buffer board) using the E3459-66507 buffer board are required.


Agilent
E5904B
IP Address = probe1
JTAG Signals
Trace Connector
21 (13, or 9) TRACE SIGNALS
16 (8 or 4) TRACEPKT
3 PIPESTAT
1 TRACESYNC
1 TRACECLK
Buffer Board
E5903-66507
Trace Connector
JTAG
Signals
Trace Multiplexer
Trace Port A
Signals
Trace Port B
Signals
Trace Port n
Signals
ETM
Port A
ETM
Port B
ETM
Port n
ARM Core 1
ARM Core 2
ARM Core n
TDI
JTAG
Controller 1
JTAG
Controller 2
JTAG
Controller n
TDO
Target Board

Collecting Trace Simultaneously from Two ARM Cores

This setup allows the user to control a multiple core system and collect two traces simultaneously. The master trace port analyzer performs all run control functions. The master trace port analyzer also collects trace information from one of the ETMs. The slave trace port analyzer does not perform run control; it only collects trace information from one additional ETM.

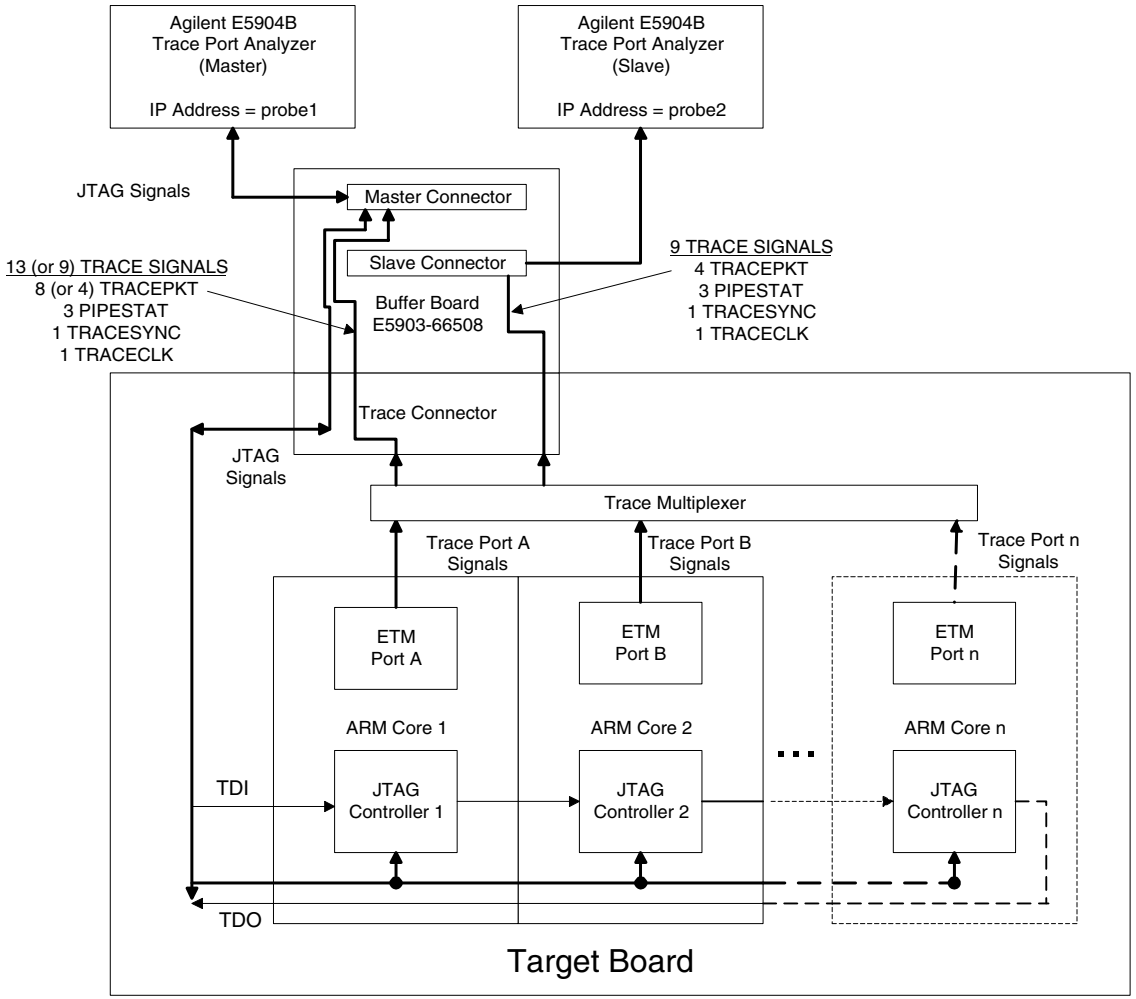
Thirteen trace signals (eight trace packet signals) from the target system are connected to the master trace port analyzer and nine trace signals (four trace packet signals) from the target system are connected to the slave trace port analyzer.

The master can handle eight trace packet signals. Therefore, the multiplexer should direct the ETM that does the most intensive read/write data tracing to the master trace port analyzer.

The slave ETM is best suited to trace code execution because it is configured for only four trace packet signals.

Two trace port analyzers and a target probe (68-pin cable and buffer board) using the E3459-66508 buffer board are required.

The user must design, implement, and control the trace multiplexer.


Agilent E5904B
Trace Port Analyzer
(Master)
IP Address = probe1
Agilent E5904B
Trace Port Analyzer
(Slave)
IP Address = probe2
JTAG Signals
Master Connector
Slave Connector
13 (or 9) TRACE SIGNALS
8 (or 4) TRACEPKT
3 PIPESTAT
1 TRACESYNC
1 TRACECLK
9 TRACE SIGNALS
4 TRACEPKT
3 PIPESTAT
1 TRACESYNC
1 TRACECLK
Buffer Board
E5903-66508
Trace Connector
JTAG
Signals
Trace Multiplexer
Trace Port A
Signals
Trace Port B
Signals
Trace Port n
Signals
ETM
Port A
ETM
Port B
ETM
Port n
ARM Core 1
ARM Core 2
ARM Core n
TDI
JTAG
Controller 1
JTAG
Controller 2
JTAG
Controller n
TDO
Target Board

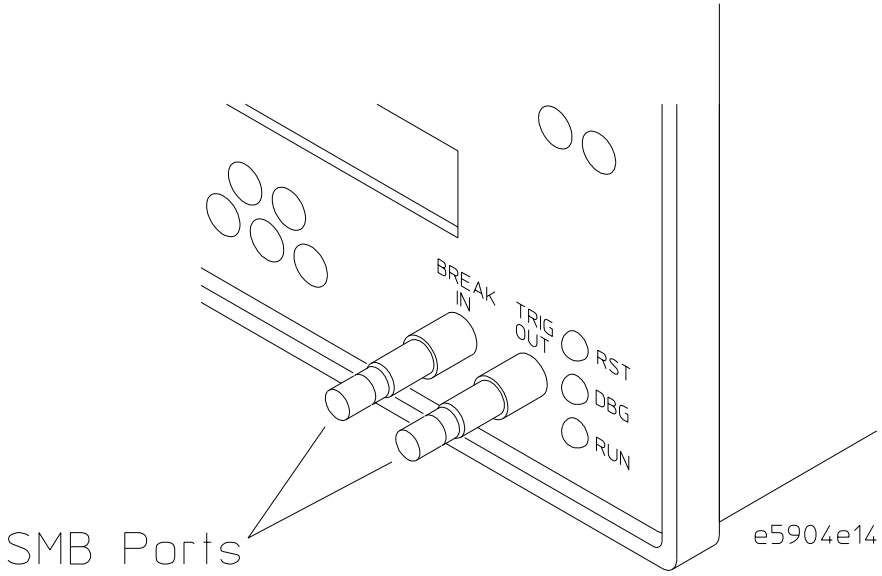
9

Coordinating Measurements with Other Test Instruments

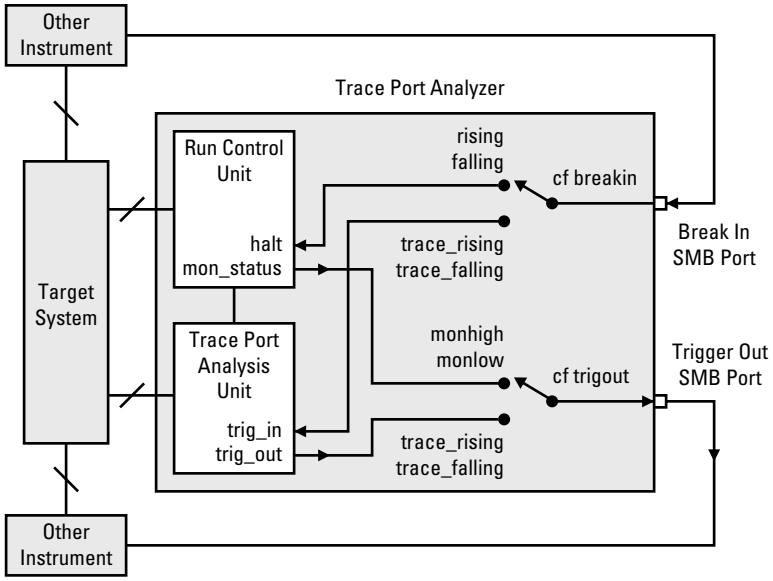
You can make coordinated measurements when you want to correlate real-time trace data from the Embedded Trace Macrocell with data captured by other test instruments (for example, a logic analyzer that captures data from other parts of your target system).

The Agilent Technologies E5904B Option 300 trace port analyzer has two SMB ports for coordinating measurements with other test instruments:

- Trigger Out SMB port.
- Break In SMB port.



By using the trace port analyzer's "trigout" and "breakin" configuration options, you can route the Trigger Out and Break In signals to either the run control unit or to the trace port analysis unit.



Receiving a Break In Signal from Another Test Instrument

You can use the trace port analyzer's Break In signal to:

- Allow another test instrument to halt processor execution (in other words, make the run control unit run in its monitor).
- Allow another test instrument to enable the trace port analysis unit.

To halt processor execution

When another test instrument detects a problem, you might want to stop processor execution, for example, to examine registers and variable values or to begin stepping through processor execution.

1. Connect the other test instrument's output to the trace port analyzer's Break In SMB port.
2. Set the trace port analyzer's "breakin" configuration item to either "rising" or "falling" (depending on whether the other test instrument outputs a rising edge or a falling edge).
3. Start the processor's execution using the run control unit.
4. Start the other test instrument's measurement.

See Also

"To configure the Break In SMB port" on page 93.

To specify when to capture trace port data

When another test instrument detects a problem, you might want to see what the processor is executing when the problem occurs.

1. Connect the other test instrument's output to the trace port analyzer's Break In SMB port.
2. Set the trace port analyzer's "breakin" configuration item to either "trace_rising" or "trace_falling" (depending on whether the other test instrument outputs a rising edge or a falling edge).
3. Start the trace port analysis unit's measurement.
4. Start the other test instrument's measurement.

See Also

"To configure the Break In SMB port" on page 93.

Driving a Trigger Out Signal to Another Test Instrument

You can use the trace port analyzer's Trigger Out signal to:

- Indicate to another test instrument when processor execution stops (in other words, when the run control unit is in its monitor).
- Indicate to another test instrument when the trace port analysis unit's trigger occurs.

To indicate when processor execution stops

You might want to do this, for example, to qualify a (synchronous) state logic analyzer's sampling clock so that it captures data only when the processor is executing the target program (and not when the debugger is using the run control unit to read and write memory locations).

1. Connect the trace port analyzer's Trigger Out SMB port to the other test instrument's input.
2. Set the trace port analyzer's "trigout" configuration item to either "monhigh" or "monlow" (depending on whether the other test instrument expects an active high or an active low signal).
3. Start the other test instrument's measurement.
4. Control the processor's execution with the run control unit.

See Also

"To configure the Trigger Out SMB port" on page 92.

To indicate when the trace port trigger occurs

You may want to use the trace port analysis unit, for example, to trigger other test instruments like oscilloscopes or logic analyzers which are looking at other parts of the target system.

1. Connect the trace port analyzer's Trigger Out SMB port to the other test instrument's input.
2. Set the trace port analyzer's "trigout" configuration item to either "trace_high" or "trace_low" (depending on whether the other test instrument expects a rising edge or falling edge to signal when the trigger occurs).
3. Start the other test instrument's measurement.
4. Run the trace port analysis unit's measurement.

See Also

"To configure the Trigger Out SMB port" on page 92.

10

Updating Firmware

If there is a newer version of firmware for the Agilent Technologies E5904B Option 300 trace port analyzer, you can update it using the procedures described in this chapter.

To display current firmware version information

1 Use the "telnet" command from a networked computer to access the trace port analyzer's built-in command interface.

2 Enter the built-in "ver -a" command to view the version information for firmware currently in the trace port analyzer.

Example

```
M>ver -a

         Copyright (c) Agilent Technologies, Inc. 1999
All Rights Reserved.  Reproduction, adaptation, or translation without prior
written permission is prohibited, except as allowed under copyright laws.

  HPE8130A Series Emulation System
    Version:   A.01.09 08Mar01
    Location:  Generics

  HPE3459B ARM7/9 JTAG Emulator
    Version:   A.05.07 12Mar01

  HPE5840B ARM7/9 Trace Port Analyzer
    Version:   A.01.00
```

To get firmware from the web

To update the firmware, you must have access to the World Wide Web and a personal computer or a workstation connected to your trace port analyzer.

1 Download the new firmware from the following World Wide Web site:

http://www.cos.agilent.com/probe/

2 Follow the instructions on the web site for installing the firmware.

To update firmware from a floppy disk

- Follow the instructions on the README file on the floppy disk.

  The firmware can be installed using either a personal computer or a workstation which can read personal computer floppy disks.

11

Solving Problems

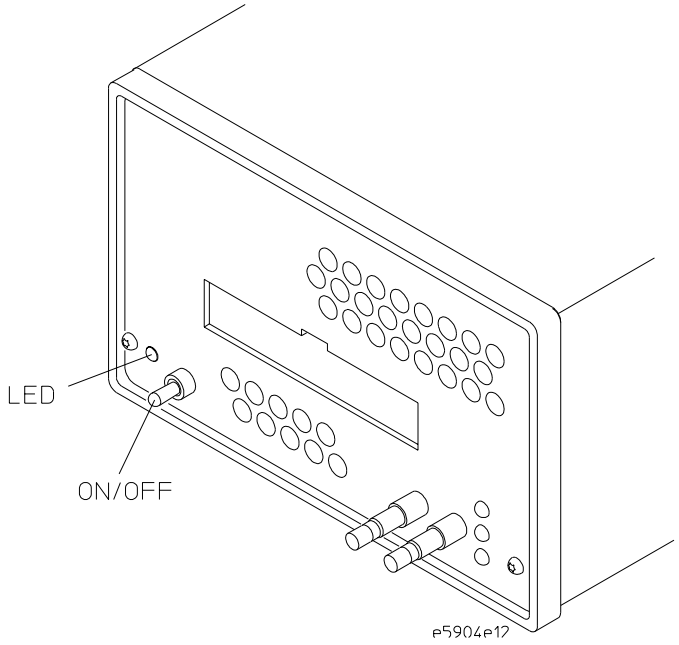
Problems with the trace port analyzer can occur in:

- The connection between the trace port analyzer and the debugger.
- The trace port analyzer itself.
- The connection between the trace port analyzer and the target system.
- The target system.

You can use the procedures in this chapter to identify the source of problems.

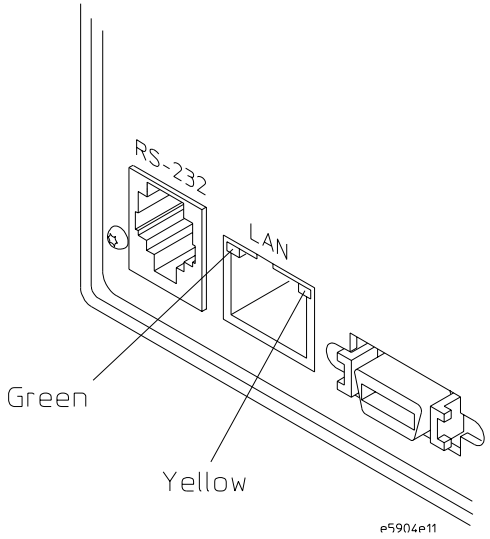
Interpreting the Trace Port Analyzer Status Lights

Power ON Light



The green LED, to the left of the power switch, is lit when the trace port analyzer is connected to a power source and the power switch is on.

LAN Status Lights

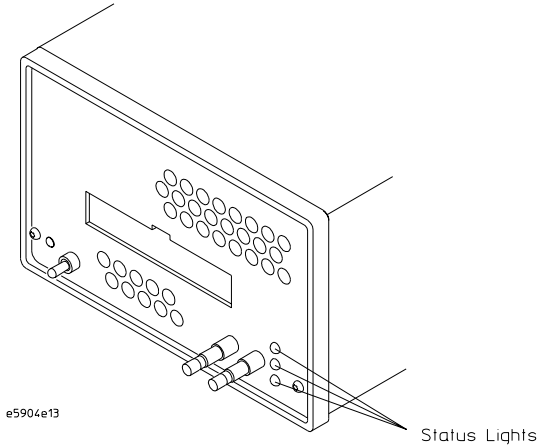


The yellow LED, on the right side of the connector, indicates LAN activity (receive or transmit).

The green LED, on the left side of the connector, is lit when the LAN interface is operating in 100Base-TX mode.

Target System Status Lights

The trace port analyzer uses status lights to communicate various modes and error conditions. The following table gives more information about the meaning of the power and target system status lights.



❍ = LED is off ● = LED is on

Power/Target System Status Lights

❍ RST ❍ DBG ❍ RUN	No power to the target system, or trace port analyzer is not connected to the target system
● RST ❍ DBG ❍ RUN	Target system is in a reset state
❍ RST ● DBG ❍ RUN	The target system processor is in Debug Mode
❍ RST ❍ DBG ● RUN	The target system processor is executing user code
❍ RST ● DBG ● RUN	Only boot firmware is good (other firmware has been corrupted)
● RST ● DBG ● RUN	The trace port analyzer can no longer control the target system. Reset the target system; then, initialize the trace port analyzer.

Verifying Trace Port Analyzer LAN Communications

Follow these steps if there are problems establishing LAN communications to the trace port analyzer from a debugger or by using telnet on a networked computer.

Step 1. Verify the physical connection

1 Make sure that the proper LAN cable is connected.

- Use a Category 5 cable if your connection is running at 100 Mbps (100BASE-TX).
- Use a Category 3 cable if your connection is running at 10 Mbps (10BASE-T).

2 With the trace port analyzer powered on, look at the LAN status lights to verify that the trace port analyzer is seeing LAN activity.

See “LAN Status Lights” on page 140. No activity indicates a problem with the LAN port or cable. Contact your network system administrator.

Step 2. Use the “ping” command on a networked computer

These instructions assume you are using a personal computer running Microsoft® Windows®. The procedure for other operating systems is slightly different.

1 Open an MS-DOS Command Prompt window, or choose Start->Run....

2 Enter the “ping” command followed by the IP address of the

trace port analyzer.

Example

```
C:\WINDOWS>ping 192.35.12.6

Pinging 192.35.12.6 with 32 bytes of data:

Reply from 15.6.253.138: bytes=32 time=1ms TTL=254
Reply from 15.6.253.138: bytes=32 time=1ms TTL=254
Reply from 15.6.253.138: bytes=32 time=1ms TTL=254
Reply from 15.6.253.138: bytes=32 time<10ms TTL=254
```

3 If ping gets replies from the trace port analyzer (but you are unable to telnet to it), try rebooting the trace port analyzer by turning its power switch off then on again.

Problems with trace port analyzer firmware could lead to situations where the LAN interface is up and running but you are not able to telnet to the trace port analyzer or, if you are able to telnet to the trace port analyzer, you are not able to enter commands.

If there are LAN connection problems

If the results of the "ping" command shows something like "100% packet loss" or "Destination host unreachable":

- ❏ Make sure that you have connected the trace port analyzer to the proper power source and that the power light is lit.
- ❏ Make sure that you wait for the power-on self test to complete before connecting.
- ❏ If you have just changed the IP address of the trace port analyzer, leave the trace port analyzer powered on and connected to the LAN for a few minutes, then try again.

  Some hubs, routers, and hosts maintain tables of IP addresses and link-level addresses. It may take a while for these tables to be updated.

- ❏ Make sure that the trace port analyzer's IP address is set up correctly.

  To do this, repeat the steps shown in "To set LAN parameters using a serial port connection" on page 56.

- ❏ If the trace port analyzer is on a different subnet than the host computer, make sure that the gateway address is set up correctly.

  The default gateway address of 0.0.0.0 does not allow the trace port analyzer to communicate with computers on other subnets.

If it takes a long time to connect to the network

- ❏ Check the subnet masks on the other LAN devices connected to your network. All of the devices should be configured to use the same subnet mask.

  Subnet mask error messages do not indicate a major problem. You can continue using the trace port analyzer.

  If there are many subnet masks in use on the local subnet, the trace port analyzer may take a very long time to connect to the network after it is turned on.

Checking the Initial Trace Port Analyzer Status

After establishing a telnet connection to the trace port analyzer, an initial status prompt of “->” or “?>” indicates a problem.

If the prompt is “->”

The "->" prompt indicates that the trace port analyzer is not connected to a target probe (which is the 68-pin cable and a buffer board) or that the firmware loaded into the trace port analyzer is not compatible with its hardware.

Try one of the following until you get a different prompt:

- ❏ If the trace port analyzer is not connected to the target probe, connect the target probe and enter the “init -c” command to re-initialize.
- ❏ Cycle power on the trace port analyzer. (Turn off target system power first.)
- ❏ Check that the proper firmware is installed by entering the “ver” command.

  The proper firmware is installed at the factory but it could accidentally be changed. If the firmware is incorrect, refer to Chapter 10, “Updating Firmware,” on page 133.
- ❏ Run the trace port analyzer performance verification tests to make sure it is working correctly.

  Refer to “Running Trace Port Analyzer Performance Verification Tests” on page 156.

If the prompt is “?>”

The "?>" prompt indicates that the trace port analyzer is having trouble communicating with the target system. The trace port analyzer doesn’t know what state the target system is in.

❑ Follow the procedure in the “Verifying Run Control Interaction with the Target System” on page 147.

Verifying Run Control Interaction with the Target System

Use the following procedure to verify that the trace port analyzer's run control port is operating properly with the target system.

Connection to the wrong target system or connection to a target system whose pins are connected backward could potentially damage the trace port analyzer.

Step 1. Initialize the trace port analyzer

1. Follow the procedure in Chapter 6, "Connecting to a Target System," on page 101.
2. Telnet to the trace port analyzer.
3. Initialize the trace port analyzer by entering the "init -c" command.

```
?>init -c
```

You can enter this command at any prompt. This command will set the default configuration settings and will display the same information as the "ver" command.

The initial prompt can be used to diagnose several common problems.

If the initial prompt is "R>", the trace port analyzer is scanning the JTAG interface correctly. Go to "Step 2. Configure the trace port analyzer" on page 149.

If the response is "!ERROR 905!"

If the response is "!ERROR 905! Driver firmware is incompatible with ID of attached device":

❏ Make sure the correct firmware is loaded into the trace port analyzer.

See "To display current firmware version information" on page 134.

If the initial prompt is "p>"

❏ Make sure that the target system is powered on and that the VTref pin on the target system header connector has the proper reference voltage.

If the initial prompt is "M>"

❏ The processor entered debug mode without the help of the trace port analyzer. Is another debugger connected?

If the initial prompt is "?>"

❏ Check TCK, TDO, TDI, TMS, and nTRST signals. Check the firmware revision.

Check for the following logic levels on the target system's debug port. The signal names are for the ARM7.

Signal Levels with the trace port analyzer in default[1] reset state

Signal Name	Level
Vcc/VTref/SPU	1.65 V - 3.6 V[2]
TDI	Toggling
TDO	Toggling
TCK	~10 MHz signal
TMS	Toggling
nSYSRST	Low
DBGACK	Low
DBGREQ	Low
nTRST	High

All other pins should be low.

[1]Default cf settings

[2]Target dependent

If the run control port signals are okay and the prompt is still "?>", refer to "If the trace port analyzer has problems controlling the target system" on page 154.

Step 2. Configure the trace port analyzer

- Configure the trace port analyzer appropriately for the target system.

  See Chapter 5, "Configuring the Trace Port Analyzer," on page 73.

  If the appropriate configuration options were previously saved with the "cfsave -s" command, you can restore them with the "cfsave -r" command.

Step 3. Enter the reset command

- Enter the “rst” command:

```
R>rst
R>
```

The "R>" prompt is a good response that indicates that nRESET is working. Go to “Step 4. Enter the run command” on page 150.

Step 4. Enter the run command

- Enter the “r” command:

```
R>r
U>
```

If the prompt after the run command is "U>" with no error messages, everything is still working correctly. Go to “Step 5. Enter the break command” on page 150.

Step 5. Enter the break command

- Enter the “b” command:

```
U>b
M>
```

If the prompt after the break command is "M>" with no error messages, everything is still working correctly. Go to “Step 6. Check register and memory access” on page 151.

If the prompt is "U>" with error messages

- ❏ If you see "!ERROR 608! Unable to break", make sure the processor type configuration option is set correctly.
- ❏ If "!ERROR 608! Unable to break" still occurs, reduce JTAG communication speed (see page 82).
- ❏ Reset (or cycle power on) the target system.
- ❏ Make sure you are using the command sequence:

```
U>rst
R>r
U>b
M>
```

  Some ARM chips have problems if JTAG commands are issued while the chip is reset. Using the "rst", "r", "b" sequence avoids this problem.

- ❏ If the problem persists, see "If the trace port analyzer has problems controlling the target system" on page 154.

Step 6. Check register and memory access

1 At the "M>" prompt, check register accesses:

```
M>reg r0
  reg r0=xxxxxxxx
M>reg r0=12345678
M>reg r0
  reg r0=12345678
M>
```

If the value read is equal to the value written, the voltage level of the chip is probably correct.

2 Before checking memory accesses, set caches and translation off.

For information on doing this, refer to the documentation for the target system.

3 Check memory accesses:

```
M>m -d4 -a4 0=11111111,22222222,33333333,44444444
M>m -d4 -a4 0..
  00000000   11111111 22222222 33333333 44444444
  00000010   00000000 00000000 00000000 00000000
  00000020   00000000 00000000 00000000 00000000
  00000030   00000000 00000000 00000000 00000000
  00000040   00000000 00000000 00000000 00000000
  00000050   00000000 00000000 00000000 00000000
  00000060   00000000 00000000 00000000 00000000
  00000070   00000000 00000000 00000000 00000000
M>
```

If the values read are equal to the values written, memory is working. Go to "Step 7. Run a short program" on page 152.

If you see memory-related problems

❑ If the value read is not equal to the value written, it implies that the memory controller may not be initialized.

Be sure the memory controller for your target system is setup correctly.

Step 7. Run a short program

To more fully test your target, you can load simple programs into memory and execute them.

1 Modify memory locations to load a short program:

```
M>m -d4 -a4 100=e2811001,00000000,eafffffc
M>reg r1=0
M>
```

In assembly language this is:

```
ADD   r1,r1,#1
NOP
B     100
```

2 Set the program counter register to the address of the short program:

```
M>reg pc=100
M>
```

NOTE: Stepping can fail if memory at the current program counter does not contain a valid instruction.

3 Step the program; then, check the register contents:

```
M>s
  pc=00000104
M>reg r1
  reg r1=00000001
M>
```

This should return "reg r1=00000001".

4 Verify that the register increments after every three steps:

```
M>s 3
  pc=00000104
M>reg r1
  reg r1=00000002
M>
```

If the program does not execute correctly

If this does not work as described, make sure “cf endian” is set correctly for your target, the memory at 100 is read/write memory, and that the memory controller is programmed correctly.

If the trace port analyzer has problems controlling the target system

The trace port analyzer might be having problems controlling the target if you see messages such as:

"!ERROR 608! Unable to break"

Or the prompt changes to "?>"

Problems controlling the target can be caused by a variety of conditions. Typically the problem is in the configuration of the trace port analyzer or the configuration of the target system.

Try the following to better control your target system:

- ❏ Decrease the JTAG communication speed. Some target systems need slower speeds to properly communicate.

  Use the **`cf speed`** command (see "To specify the JTAG clock speed" on page 82).

- ❏ Check the trace port analyzer configuration settings.

  Enter the **`cf`** command to display the configuration settings (see "Using the Built-In "cf" Command" on page 75).

- ❏ Check that the trace port analyzer is not restricted to real-time runs.

  If you are using a telnet connection or a debugger command file, use the **`cf rrt=no`** command.

  Restricting to real-time runs will not allow you to access memory or registers while the target system program is running. By setting this option to "no", you will be able to access the memory and registers while the target system program is running.

- ❏ Check that the target system processor is configured.

  Some devices under test require configuration registers on the processor to be initialized before the trace port analyzer can properly communicate with the target system.

  For example, some processors need their memory controllers initialized.

  To initialize the target processor, either run the target system from reset (if you have a BOOT ROM) or define a series of trace port analyzer commands to initialize the target system.

- ❏ Check that the proper firmware is installed by entering the "ver" command (see "To display current firmware version information" on page 134).

  The proper firmware is installed at the factory but it could accidentally be changed. If the firmware is incorrect, refer to Chapter 10, "Updating Firmware," on page 133.

Running Trace Port Analyzer Performance Verification Tests

In addition to the powerup tests, there are several additional performance verification (PV) tests available.

These tests can be performed using either a LAN connection or a serial port (RS-232) connection.

Step 1. Prepare for the performance verification tests

You will need the Agilent E5903-66509 PV board and an SMB cable to perform the performance verification tests. The PV board is supplied with the Agilent E5904 Option 300 trace port analyzer; the SMB cable is not.

1. End any debugger sessions.
2. Power OFF the target system.
3. Power OFF the trace port analyzer.
4. Disconnect the trace port analyzer from the target system.

CAUTION: If the trace port analyzer is not disconnected from the target system and the performance verification tests are run, the Target Board Adapter Feedback Test can damage components on the target system.

5. Connect the E5903-66509 PV board to the 68-pin cable of the trace port analyzer.
6. Connect an SMB (f) to SMB (f) cable (such as Agilent 16532-61601) from the "Break In" connector to the "Trigger Out" connector on the trace port analyzer.

   If you aren't concerned about these signals, you may omit this step and

ignore any related test failures.

7 Turn the trace port analyzer on again.

8 Access the trace port analyzer's built-in command interface.

If you're using a LAN connection, you can **`telnet`** to the trace port analyzer from a computer on the network and enter commands (see "To "telnet" to the trace port analyzer" on page 68).

If you're using a serial port (RS-232) connection, you can connect a terminal emulator or an actual terminal to the trace port analyzer and use it to enter commands (see "To set LAN parameters using a serial port connection" on page 56).

Step 2. Enter the "pv" command

Options available for the **`pv`** command are explained in the help screen displayed by typing **`help pv`** or **`? pv`** at the prompt.

1 Enter the **`pv 1`** command.

The results on a good system, with the trigger out and break in SMBs connected, should look similar to the following.

```
p>pv 1

  Testing: HPE8130A Series Emulation System
    Test  1: Powerup PV Results                              Passed!
    Test  2: Emulation Module Port Feedback Test             Passed!
    Test  3: Run Control FPGA Test                           Passed!
    Test  4: Run Control Clock Test                          Passed!
    Test  5: Break In and Trigger Out SMB Feedback Test      Passed!
  Testing: HPE3459B ARM7/9 JTAG Emulator
    Test  1: Trace Board Feedback Test                       Passed!
    Test  2: Target Probe Feedback Test                      Passed!
  PASSED  Number of tests: 1           Number of failures: 0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written permission is prohibited, except as allowed under copyright laws.

  HPE8130A Series Emulation System
    Version:   A.01.05 Dec 15 2000
    Location:  Generics

  HPE3459B ARM7/9 JTAG Emulator
    Version:   B.05.05 Dec 06 2000

  HPE5840B ARM7/9 Trace Port Analyzer
    Version:   A.01.00 Jan 08 2001

R>
```

2 If a performance verification test fails, enter the **`pv -v3 1`** command.

Details of the failure can be seen by entering the "pv" command again with a verbose level of 3.

If the powerup PV results test fails

Failure of the Powerup PV Results test indicates a hardware problem with the trace port analyzer.

❑ Contact Agilent Technologies for assistance (see "Contacting Agilent Technologies" on page 161).

If the emulation module port feedback test fails

Failure of the Emulation Module Port Feedback Test indicates a hardware problem with the trace port analyzer.

❑ Contact Agilent Technologies for assistance (see "Contacting Agilent Technologies" on page 161).

This test exercises the hardware which drives the connection to the trace port analyzer.

If the run control FPGA test fails

Failure of the Run Control FPGA Test indicates a hardware problem with the trace port analyzer.

❏ Contact Agilent Technologies for assistance (see "Contacting Agilent Technologies" on page 161).

If the trace port analyzer fails this test, it may have been damaged by electrostatic discharge through the target cable. To prevent such damage in the future, follow standard ESD preventive practices.

If the run control clock test fails

Failure of the Run Control Clock Test indicates a hardware problem with the trace port analyzer.

❏ Contact Agilent Technologies for assistance (see "Contacting Agilent Technologies" on page 161).

If the trace port analyzer fails this test, it may have been damaged by electrostatic discharge through the target cable. To prevent such damage in the future, follow standard ESD preventive practices.

If the break in and trigger out SMB feedback test fails

If the Break In and Trigger Out SMB Feedback Test fails:

❏ Make sure you have connected a good cable between the two SMB connectors.

❏ If the cable is good, contact Agilent Technologies for assistance (see "Contacting Agilent Technologies" on page 161).

If the trace board feedback test fails

Failure of the Trace Board Adapter Feedback Test indicates a hardware problem with the trace port analyzer.

❏ Contact Agilent Technologies for assistance (see "Contacting Agilent Technologies" on page 161).

If the target probe feedback test fails

Failure of the Target Probe Feedback Test indicates a hardware problem with the trace port analyzer.

❏ Make sure the target probe (that is, the 68-pin cable and the appropriate buffer board) is connected to the trace port analyzer.

❏ Contact Agilent Technologies for assistance (see "Contacting Agilent Technologies" on page 161).

Contacting Agilent Technologies

If the trace port analyzer still does not work after following the troubleshooting steps in this chapter:

1. Write down the target processor version, the trace port analyzer firmware version, and the trace port analyzer model number (Agilent Technologies E5904B Option 300).
2. Call your nearest Agilent Technologies sales or service office.

   To locate a sales or service office near you, go to the world-wide web site:

   http://www.tm.agilent.com

   and select Contact Us.

12

Characteristics

This chapter describes the following characteristics of the Agilent Technologies E5904B Option 300 trace port analyzer:

- Input/output electrical characteristics.
- Run control unit characteristics.
- Trace port analysis characteristics.
- Environmental characteristics.

Input/Output Electrical Characteristics

Trigger Out SMB Port

With a 50 Ω load, a logic high is ≥ 2.0 V, and a low is ≤ 0.4 V. The output function is selectable (see "To configure the Trigger Out SMB port" on page 92).

Break In SMB Port

Edge-triggered TTL level input, 20 pF, with 4.6 kΩ to ground in parallel. Maximum input: +5 V to -5 V when the trace port analyzer is powered OFF; +10 V to -5 V when the trace port analyzer is powered ON. Input function is selectable (see "To configure the Break In SMB port" on page 93).

Communication Ports

Serial Port

RJ12 connector (DB9-to-RJ12 adapter and serial cable included). RS-232 DCE to 115.2 kbaud.

IEEE 802.3 Type 10/100Base-TX LAN Port

RJ-45 connector, is compatible with both 10 Mbps (10Base-T) and 100 Mbps (100Base-TX) twisted-pair ethernet LANs.

Power Supply

Input. 100-240 V, 1.0 A, 50/60 Hz, IEC 320 connector.

Output. 12 V, 3.3 A

CAT I (Mains isolated).

Run Control Unit Characteristics

Processor Compatibility

The Agilent Technologies E5904B Option 300 trace port analyzer supports several ARM7/9 processors. For the complete list, see "To set the type of ARM processor" on page 79.

Electrical Characteristics

TDO, DBGACK, RTCK Input Characteristics							
Signal	**Symbol**	**1/3 Vref**		**1/2 Vref**		**2/3 Vref**	
		Min	**Max**	**Min**	**Max**	**Min**	**Max**
TDO, DBGAC, RTCK	Vih	0.5 Vref	5.1 V	0.65 Vref	5.1 V	0.8 Vref	5.1 V
	Vil	-0.1V	0.2 Vref	-0.1 V	0.35 V	-0.1 V	0.5 Vref
	Ib (Bias)	± 15 uA					
	Rin	4.7 kΩ pullup to Vref					
	Cin	TDO = 75 pF, DBGACK = 95 pF, RTCK = 80 pF					

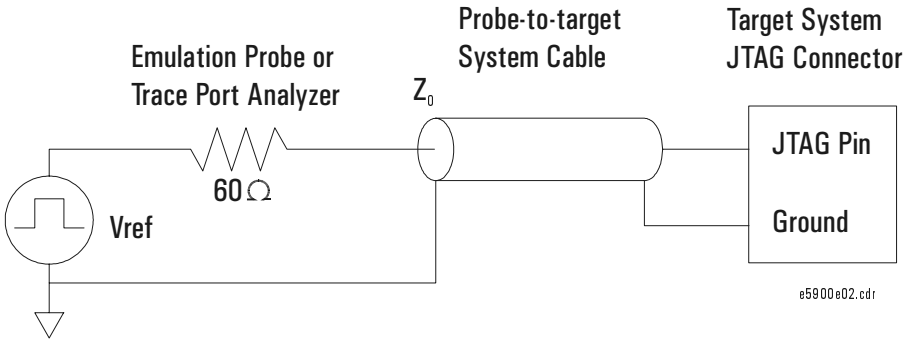
VTref, SRST Input Characteristics			
Signal	**Symbol**	**Min**	**Max**
VTref[1]	Vin	1.65 V	3.6 V
	Rin	25 kΩ pulldown to ground	
$\overline{\text{SRST}}$	Rin (inactive)	4.7 kΩ pullup to Vref	
	Rin (active)	12 Ω pulldown to ground	
	Cout		200 pF
	Vin		5.5 V

[1] VTref is used to determine the target power status and the reference for input threshold and output voltage swings. The trace port analyzer does not draw power from this source.

Output Signal Characteristics		
Signal	**Symbol**	**Condition**
TDI, TCK, TMS, $\overline{\text{TRST}}$, DBGRQ	Voh/Ioh	66 Ω ± 15 Ω to Vref
	Vol/Iol	66 Ω ± 15 Ω to 0.2 V

Output Model

This is the model of output drive to TDI, TCK, TMS, TRST and DBGRQ.



Note: Z_o = 66 Ω in the diagram above.

Trace Port Analysis Unit Characteristics

For the characteristics of the trace port analysis unit, see:

- "Signal Requirements" on page 38.
- "Buffer Board—Required Voltage Levels" on page 39.
- "Loading Effects" on page 40.

Environmental Characteristics

Temperature	Operating: +5 degrees to +40 degrees C (+41 to +104 degrees F) Non-operating: -40 degrees to +70 degrees C (-40 to +158 degrees F).
Relative Humidity	15% to 95%
Pollution Degree	Pollution degree 2: Normally only dry non-conductive pollution occurs. Occasionally a temporary conductivity caused by condensation may occur.
Altitude	Operating or non-operating: 4600 m (15 000 ft.).
For indoor use only.	

EMC

	Performance Criteria
IEC 61326-1:1997+A1:1998 / EN 61326-1:1997+A1:1998	
CISPR 11:1990 / EN 55011:1991– Group 1 Class A	A See Note
IEC 61000-4-2:1995+A1:1998 / EN 61000-4-2:1995 (ESD 4kV CD, 8kV AD)	A
IEC 61000-4-3:1995 / EN 61000-4-3:1995 (3V/m 80% AM)	A
IEC 61000-4-4:1995 / EN 61000-4-4:1995 (EFT 0.5kV line-line, 1kV line-earth)	A
IEC 61000-4-6:1996 / EN 61000-4-6:1996 (3V 80% AM, power line)	A
Australia/New Zealand: AS/NZS 2064.1	
Canada: ICES-001:1998	

Safety

IEC 61010-1:1990+A1:1992+A2:1995 / EN 61010-1:1994+A2:1995
Canada: CSA C22.2 No. 1010.1:1992
USA: UL 3111-1:1994 {optional}

Additional Information:

The product herewith complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC (including 93/68/EEC) and carries the CE Marking accordingly (European Union).

Performance Criteria:
A Pass - Normal operation, no effect.
B Pass - Temporary degradation, self recoverable.
C Pass - Temporary degradation, operator intervention required.
D Fail - Not recoverable, component damage.

Note:
The target probes (cable plus buffer board) are ESD sensitive. Use standard ESD preventive practices to avoid component damage.

13

Service Guide

To get replacement parts

The following table lists some parts that may be replaced if they are damaged or lost. The part numbers are subject to change. Contact your nearest Agilent Technologies sales office for further information (see "Contacting Agilent Technologies" on page 161).

Replacement assemblies

Part number	Description
0950-3043	Power supply for trace port analyzer (marked F1044B)
E3483-68700	Power supply ferrite kit
E5903-61602	68-pin cable
E5903-66507	ARM buffer board
E5903-66508	ARM dual ETM buffer board
E5903-66509	PV board
E8130-68702	Serial cable and adapter

NOTE: See the figure on page 5 for an illustration of most of these replacement parts.

To exchange a faulty assembly for a repaired and tested assembly

The following item has been set up on the Agilent Technologies exchange assembly program. You can exchange a faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. The cost is significantly less than that of a new assembly.

Exchange assemblies

Part number	Description
E5840-69501	Rebuilt trace port analyzer for ARM (accessories not included)

To return a part to Agilent Technologies for service

1. Follow the procedures in the "Solving Problems" chapter to make sure that the problem is caused by a hardware failure and not by configuration or cabling problems.
2. Get the address of the nearest Agilent Technologies service center.

   See "Contacting Agilent Technologies" on page 161.
3. Package the part and send it to the Agilent Technologies service center.

   Keep any parts which you know are working. For example, if only a cable is broken, keep the trace port analyzer.
4. When the part has been replaced, it will be sent back to you.

   The unit returned to you will have the same serial number as the unit you sent to Agilent Technologies.

   In some parts of the world, on-site repair service is available. Ask an Agilent Technologies sales or service representative for details.

To clean the instrument

If the instrument requires cleaning:

1. Remove power from the instrument.
2. Clean the instrument using a soft cloth that has been moistened in a mixture of mild detergent and water.
3. Make sure that the instrument is completely dry before reconnecting it to a power source.

D

debug port A hardware interface designed into a microprocessor that allows developers to control microprocessor execution, set breakpoints, and access microprocessor registers or target system memory using a tool like the emulation probe.

device under test Another name for a target system under development.

H

hostname A name that is associated with the IP address of a device on the network.

I

IP address An address, in integer dot notation (for example, 15.6.240.253), that is given to a device on the network.

J

JTAG port See *debug port*.

JTAG interface unit See *run control unit*.

L

LAN name See *hostname*.

N

N-trace A method for embedded processor cores in ASICs to output information about program execution using relatively few pins on the ASIC.

R

run control unit A device that connects to a microprocessor's debug port to provide run control features like: starting/stopping program execution, single-stepping through programs, and modifying registers and memory contents.

T

target system The device under test that is being developed and debugged.

threshold voltage The level at which voltages above are logic "highs" (1) and voltages below are logic "lows" (0).

trace port analyzer A tool that collects an N-trace port's execution information and presents it to a software debugger.

trigger specification A set of conditions that must be true before the instrument triggers.

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DECLARATION OF CONFORMITY

According to ISO/IEC Guide 22 and CEN/CENELEC EN 45014

Manufacturer's Name: Agilent Technologies, Inc.
Manufacturer's Address: 1900 Garden of the Gods Road
Colorado Springs, Colorado
80907 U.S.A.

Declares, that the product

Product Name: Trace Port Analyzer

Model Number: E5904B (E3483B)

Product Options: This declaration covers all options of the above product(s).

Conforms with the following product standards:

EMC	Standard	Limit
	IEC 61326-1:1997+A1:1998 / EN 61326-1:1997+A1:1998	
	CISPR 11:1990 / EN 55011:1991	Group 1 Class A [1]
	IEC 61000-4-2:1995+A1:1998 / EN 61000-4-2:1995	4kV CD, 8kV AD
	IEC 61000-4-3:1995 / EN 61000-4-3:1995	3V/m, 80-1000 MHz
	IEC 61000-4-4:1995 / EN 61000-4-4:1995	0.5kV signal lines, 1kV power lines
	IEC 61000-4-6:1996 / EN 61000-4-6:1996	3V, 0.15-80 MHz
	Canada: ICES-001:1998	
	Australia/New Zealand: AS/NZS 2064.1	
Safety	IEC 61010-1:1990+A1:1992+A2:1995 / EN 61010-1:1993+A2:1995	
	Canada: CSA C22.2 No. 1010.1:1992	

Conformity / Supplemental Information:

The product herewith complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC (including 93/68/EEC) and carries the CE Marking accordingly (European Union).

[1] The product was tested in a typical configuration with Agilent Technologies test systems.

Date: 8/24/2000

Name

Ken Wyatt / Product Regulations Manager

For further information, please contact your local Agilent Technologies sales office, agent or distributor.

Product Regulations

EMC	IEC 61326-1:1997+A1:1998 / EN 61326-1:1997+A1:1998	Performance Criteria
	CISPR 11:1990 / EN 55011:1991– Group 1 Class A	
CE	IEC 61000-4-2:1995+A1:1998 / EN 61000-4-2:1995 (ESD 4kV CD, 8kV AD)	A (See Note)
ISM 1-A	IEC 61000-4-3:1995 / EN 61000-4-3:1995 (3V/m 80% AM)	A
	IEC 61000-4-4:1995 / EN 61000-4-4:1995 (EFT 0.5kV line-line, 1kV line-earth)	A
	IEC 61000-4-6:1996 / EN 61000-4-6:1996 (3V 80% AM, power line)	A
N10149	Australia/New Zealand: AS/NZS 2064.1	
	Canada: ICES-001:1998	

Safety	IEC 61010-1:1990+A1:1992+A2:1995 / EN 61010-1:1994+A2:1995
	Canada: CSA C22.2 No. 1010.1:1992
	USA: UL 3111-1:1994 {optional}

Additional Information:

The product herewith complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC (including 93/68/EEC) and carries the CE Marking accordingly (European Union).

Performance Criteria:

A Pass - Normal operation, no effect.

B Pass - Temporary degradation, self- recoverable.

C Pass - Temporary degradation, operator intervention required.

D Fail - Not recoverable, component damage.

Note:

The target probes (cable plus buffer board) are ESD sensitive. Use standard ESD preventive practices to avoid component damage.

Sound Pressure Level N/A

Safety Notices

This apparatus has been designed and tested in accordance with IEC Publication 1010, Safety Requirements for Measuring Apparatus, and has been supplied in a safe condition. This is a Safety Class I instrument (provided with terminal for protective earthing). Before applying power, verify that the correct safety precautions are taken (see the following warnings). In addition, note the external markings on the instrument that are described under "Safety Symbols."

Warnings

• Before turning on the instrument, you must connect the protective earth terminal of the instrument to the protective conductor of the (mains) power cord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. You must not negate the protective action by using an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.

• Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short-circuited fuseholders. To do so could cause a shock or fire hazard.

• If you energize this instrument by an auto transformer (for voltage reduction or mains isolation), the common terminal must be connected to the earth terminal of the power source.

• Whenever it is likely that the ground protection is impaired, you must make the instrument inoperative and secure it against any unintended operation.

• Service instructions are for trained service personnel. To avoid dangerous electric shock, do not perform any service unless qualified to do so. Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

• Do not install substitute parts or perform any unauthorized modification to the instrument.

• Capacitors inside the instrument may retain a charge even if the instrument is disconnected from its source of supply.

• Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

• Do not use the instrument in a manner not specified by the manufacturer.

To clean the instrument

If the instrument requires cleaning: (1) Remove power from the instrument. (2) Clean the external surfaces of the instrument with a soft cloth dampened with a mixture of mild detergent and water. (3) Make sure that the instrument is completely dry before reconnecting it to a power source.

Safety Symbols

Instruction manual symbol: the product is marked with this symbol when it is necessary for you to refer to the instruction manual in order to protect against damage to the product..

Hazardous voltage symbol.

Earth terminal symbol: Used to indicate a circuit common connected to grounded chassis.

Agilent Technologies Inc.
P.O. Box 2197
1900 Garden of the Gods Road
Colorado Springs, CO 80901-2197, U.S.A.

Notices

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1900 Garden of the Gods Road
Colorado Springs, CO 80907 USA

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